FET Technology and Application

An Introduction

Edwin S. Oxner

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Preface

In 1975 there was little excitement in discrete silicon field-effect transistors (FETs). At best the market was considered to be "mature." The few manufacturers who maintained a presence in the field found their market share growing only as competitors dropped out.

On the surface, the discrete FET appeared to be sliding into obscurity simply because few graduating engineers who were entering industry had studied the technology; hence, because of their lack of familiarity, they were unaware of its potential.

If we had reviewed the commercially available discrete FET technology of that day (remembering that we are focusing on discrete *silicon* FETs, *not* gallium arsenide FETs), we would have found the junction FET (JFET) and two types of MOSFET—the classic planar type and a newer type of metal-oxide semiconductor called double-diffused, or DMOS. All three were small-signal devices available either as n-type or p-type.

Despite the lack of excitement in small-signal FETs, there were, nonetheless, certain basic advantages inherent within the technology that needed to be exploited. Among those that we examine in depth in this book are the high-speed switching characteristics, the linear transfer characteristic that offers opportunities for low distortion, and the high input, or gate, impedance. None of these desirable traits is possible with the ubiquitous bipolar transistor.

Indeed, those working in the small-signal arena didn't appreciate what they were missing because of their unfamiliarity

with FETs. And those working in the large-signal, or power field-using bipolar technology—had no realization of what lay ahead.

In late 1976, October to be exact, the FET burst into prominence that today is eclipsing that of the heretofore ubiquitous bipolar transistor! The power MOSFET was commercially introduced. Within four years of that historic date, at least a dozen semiconductor firms were offering MOSPOWER field-effect transistors.

Never has a discrete semiconductor grown in both popularity and application as quickly as the power MOSFET. Additionally, never has the semiconductor industry seen the spawning of so many new technologies based on the fundamentals of the power MOSFET. Whereas in 1975 the silicon FET was considered a mature industry with no foreseeable growth, today the silicon power FET is poised to leap well beyond whatever had been envisioned for the bipolar transistor market.

Because of the exploding popularity of *all* FETs and the unfortunate lack of understanding of FET principles, FET terminology, or FET applications, this text offers an easy-to-understand primer that should help broaden the reader's knowledge of this exciting technology.

The material in the text originated from class notes that I used in teaching at Siliconix. Some of the participants in my class were engineers, but many were not. I learned some years ago that when you need to understand a complex subject, a children's encyclopedia, where simple explanations abound, is a good place to start. Given the disparate identities among my students, offering simple phenomenological explanations was a welcome relief to all.

Consequently, I have purposely refrained from mathematical derivations to create models. Instead I have tried to create word pictures, a phenomenological understanding of how FETs work—a style that, hopefully, will benefit everyone.

I have relied extensively on equations to define certain principles, but, to keep it simple, I offer no derivations. The reader must either accept the equations by faith or dig elsewhere for proof. Opportunity to dig is provided in the references that conclude each chapter.

This book takes a broad-brush sweep across every type of FET and MOS-insulated-gate transistor popular at the time of this writing. The object of this book is threefold: (1) to provide the reader with some insights into the many styles of FET being used, (2) to offer a rudimentary understanding of their

operation and performance, and (3) to explain the complex terminology familiar among professionals, that defines the various FET parameters. To achieve these goals I give only a superficial analysis of their operation. Don't seek for depth, you won't find it here.

Additionally, I tried to explain the many symbols, characteristics, and parameters found on the typical data sheet: what they mean and how they interact.

Similarly, in Chapters 8, 9, and 10, it is now impossible to be thorough; there are simply too many diverse applications. My intent is to provide the reader with an appreciation of how and where FETs are used.

I hope that my attempt to fulfill these goals will rended some comfort to the reader who labors surrounded by a company of experts.

This book could not have reached you had it not been for the support of my family, and in particular, my wife Carol, who, having once again seen me sequestered in my office, graciously left me to "do my thing." Furthermore, my heartfelt thanks go to many of my engineering associates at Siliconix who gave invaluable support when asked. I am especially indebted to two colleagues: Richard Williams, who carefully and critically proofed the manuscript, offering many excellent suggestions, and Robin Chirico, who patiently taught me how to use the INTERLEAF* computer, which I employed to create the graphics throughout this book. But, this is *my* book; if you have any criticism, aim it at me.

Edwin S. Oxner

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Identifying the Family of FETs

1.1 Introduction

This chapter introduces the reader to all the field-effect transistors, or FETs, that we cover in this book; in addition, it offers a rudimentary, *phenomenological* understanding of how FETs operate.

Despite the plethora of both small-signal and power FETs, there are only two basic modes of operation. These operational modes are called the *depletion mode* and the *enhancement mode*.

Depletion-mode FETs are those whose drain current is reduced, or depleted, by the application of a gate potential whose polarity is *opposite* that of the drain voltage. Conversely, the enhancement-mode FET offers an increasing drain current when the polarity of the gate potential *matches* that of the drain voltage.

Within the family of FETs, shown in Figure 1.1, we have two major classifications: the junction FET, more commonly called the JFET, and the metal-oxide-semiconductor field-effect transistor, more commonly called a MOSFET. The JFET is classified as a depletion-mode FET, whereas the MOSFET can be designed to operate as either a depletion-mode or an enhancement-mode FET.

We could continue to embellish Figure 1.1, showing the many variants possible with both JFETs and MOSFETs, but we will not. Instead, this chapter offers brief descriptions and identifies where each best fits into the classification.

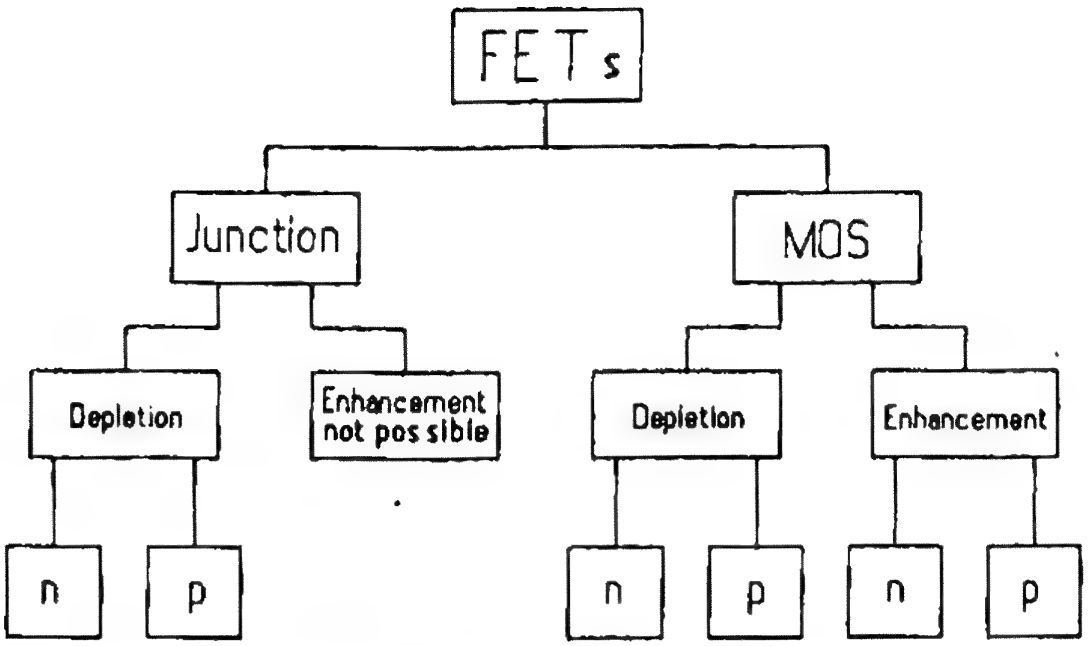


Figure 1.1 The family of FETs showing the two major classifications. Note that a JFET cannot operate in the enhancement region.

Before we continue, we need to be aware that a depletion-mode MOSFET can frequently act and perform as an enhancement-mode MOSFET, but the enhancement-mode MOSFET cannot operate as a depletion-mode MOSFET.

There are several semiconductor materials suitable for the manufacture of FETs. For example, silicon, germanium, and gallium arsenide have been, or are being used. This text considers only FETs manufactured from silicon. No FETs are made using germanium.

1.2 Small-Signal JFETs

The basic operating principle of depletion-mode JFETs may be easily understood if we first review how the depletion fields are manipulated in a p-n diode.

1.2.1 Principles of p-n Diode Operation

The simple p-n junction diode, depicted in Figure 1.2, consists of a reasonably abrupt transition from p- to n-type semiconductor. This transition is brought about, to a great extent by the

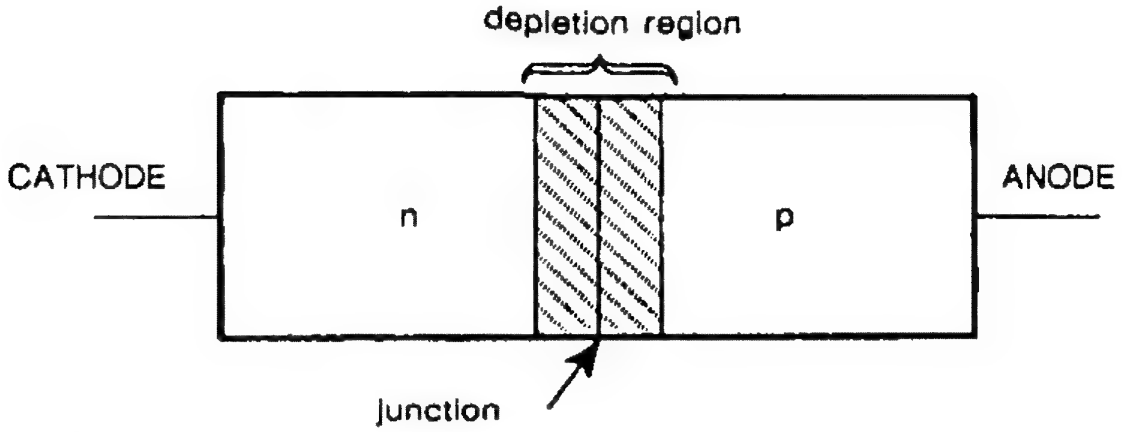


Figure 1.2 The simple pn junction showing the potential-barrier (depletion) region resulting from the interactions of electron and holes immediately adjacent to the interface.

nature of the doping process as well as by the procedure used in fabrication. The p-region, called the acceptor, may be boron-doped semiconductor, whereas the n-region, called the donor, may be either arsenic or phosphorus-doped semiconductor.

In the p-region we have a lack of free electrons, whereas in the n-region there is an abundance. If we were to consider the valence of the boron-doped (p) silicon atom, we would notice that electrons are missing from the outer shell. We identify the locations at which no electrons exist in the outer orbit as holes. Conversely, an arsenic or phosphorus-doped (n) silicon atom has an excess of free electrons.

Immediately about the p-n interface of the junction diode the free electrons in the n-region jump the transition, filling the available holes in the p-region. The resulting regions in the immediate proximity of the interface become depleted of free carriers. The p-region is depleted of hole carriers; the n-region, depleted of electron carriers. This region bordering the p-n interface is identified as the *depletion* region. This n-to-p barrier "jumping" does not continue indefinitely, or until no free electron carriers exist. A counteracting electric field, called the *Fermi level*, quickly brings the reaction into equilibrium, halting further excursions of n-electrons into the p-region.

The Depletion Region

Carriers generally do not move across or through depletion regions. As the name implies, a depletion region is depleted of carriers (whether the carriers be electrons [n] or holes [p]

necessary for conduction). How these depletion regions are manipulated in the p-n diode forms the substance of how a JFET operates.

At the p-n interface this potential-energy barrier or depletion region exists in both the p- and n-doped regions. The extent of the depletion region is dependent on the concentration of holes within the p-region as well as electrons within the n-region. Where the lesser concentration is, we will find the greater depletion area. Consequently, we find that the depletion ratio across the p-n interface is a function of the ratio of the doping densities.

For the typical p-n silicon diode this potential-energy barrier amounts to approximately 0.6 V. This means that to force carriers to jump the gap, we need to impress at least 0.6 of a volt (V_{bi}) of forward bias across the pn junction (viz., + on the p, or anode; − on the n, or cathode).

1.2.2 The Analogy to JFET Performance

All JFETs base their operation on the movement of the depletion field.

What happens if we apply a potential across the p-n diode in such a manner as to reverse-bias the junction? Remembering that like charges repel and unlike charges attract, we would expect all free carriers, whether they be holes (acting as positive charges) or electrons (which are negative charges), to be influenced according to this fundamental law. That is, negative charges would be attracted to a positive potential; positive charges to a negative potential. The result would be a greatly enlarged depletion region, as shown in Figure 1.3.

This depletion width may be calculated using a derivative of Poisson's equation.

$$W_d = \frac{(V_{bi} + V_{gs})^{1/2}}{K_1 N_c} \qquad (1.1)$$

where

V_{bi} = "built-in" junction potential
V_{GS} = applied bias
K_1 = constant
N_c = carrier concentration

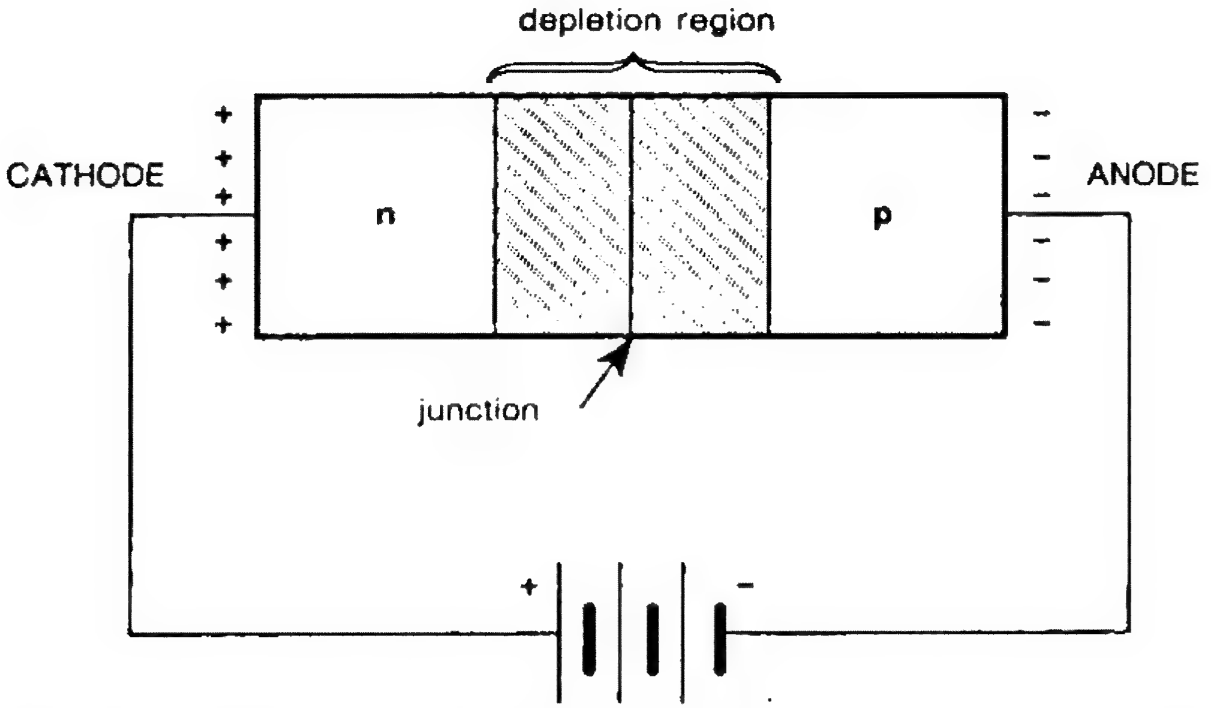


Figure 1.3 The simple pn junction showing the expanded depletion region caused by reverse bias.

We can now merge our visualization of the p-n diode with that of the JFET by placing two electrodes across either the n-doped (for an n-channel JFET) or p-doped (for a p-channel JFET) region as shown in Figure 1.4.

Current conduction between these two electrodes, which we may interchangeably call "source" and "drain," is uninhibited aside from the resistivity of the channel of doped silicon.

In a JFET the channel conductance is decreased as we increase the width of the depletion region, which immediately suggests that V_{GS} has direct control over channel conductance and thus over channel current. The effect of gate bias (V_{GS}) is shown in Figure 1.5a.

Before we continue, we need to remember that we control a JFET with a *reverse* gate-bias potential. If we were to forward bias the gate beyond the natural potential-energy barrier voltage, we would see a marked and sudden increase in gate current, as shown in Figure 1.5b.

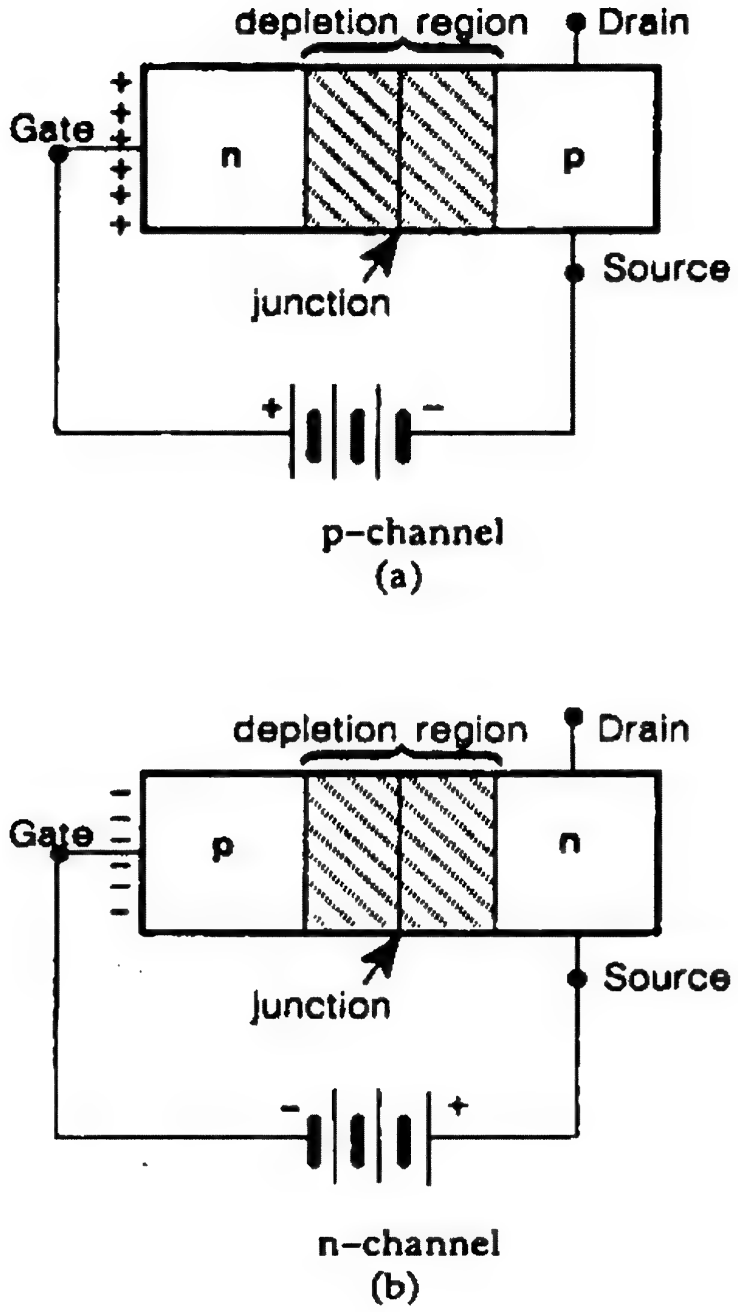
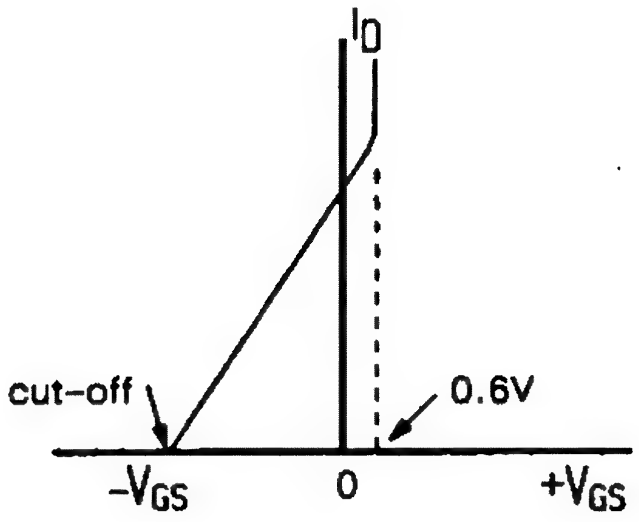


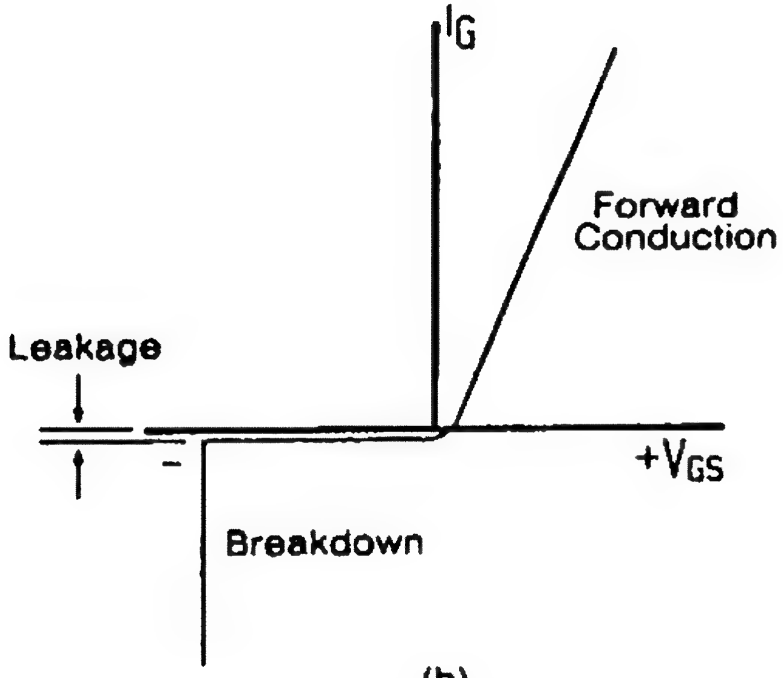
Figure 1.4 The rudimentary p-channel (a) and n-channel (b) JFET. The pn junction of the simple diode becomes the gate-channel junction of the JFET. Reverse gate bias depletes the channel, restricting current flow.

1.3 Small-Signal MOSFETs

Likewise, we can gain an appreciation of the operation of a MOSFET by reviewing how charges are distributed on a capacitor



(a)



(b)

Figure 1.5 (a) The transfer characteristics, showing the effect of gate-source bias on drain (or channel) current. (b) A forward-biased pn junction passes unlimited gate current once the potential barrier has been overcome (~0.6 V).

1.3.1 The MOS Capacitor

MOSFETs differ from junction FETs (JFETs) not only in performance but in design, as shown in Figure 1.6. Although the MOSFET performs similarly to the JEFT, it operates on a some-

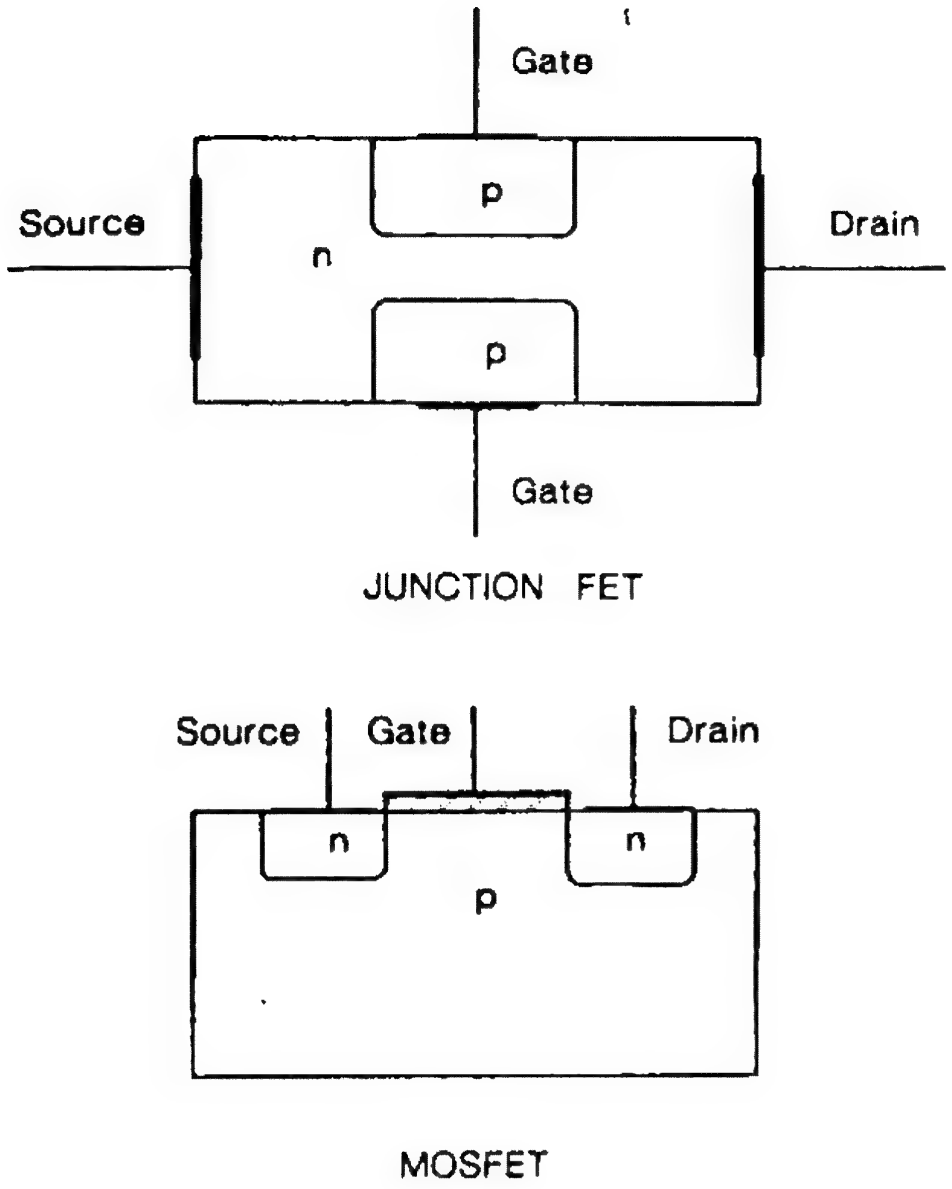


Figure 1.6 Comparison of the JFET and the enhancement-mode MOSFET. Note that the MOSFET does not have a *diffused* gate. Current conduction between source and drain is inhibited by the np/pn junctions.

what different principle. Where the JFET has a *diffused* gate embedded in the silicon channel, which, in normal operation appears as a reverse-biased pn junction diode, the MOSFET gate is electrically isolated from the channel. A MOS capacitor exists whose two plates are the gate and the silicon region beneath the insulating gate oxide, the dielectric generally being silicon dioxide. For the MOSFET, the depletion regions are induced by capacitor action (see Figure 1.7). Whatever charge is placed on one plate (gate) induces an equal and opposite charge on the opposing plate (channel).

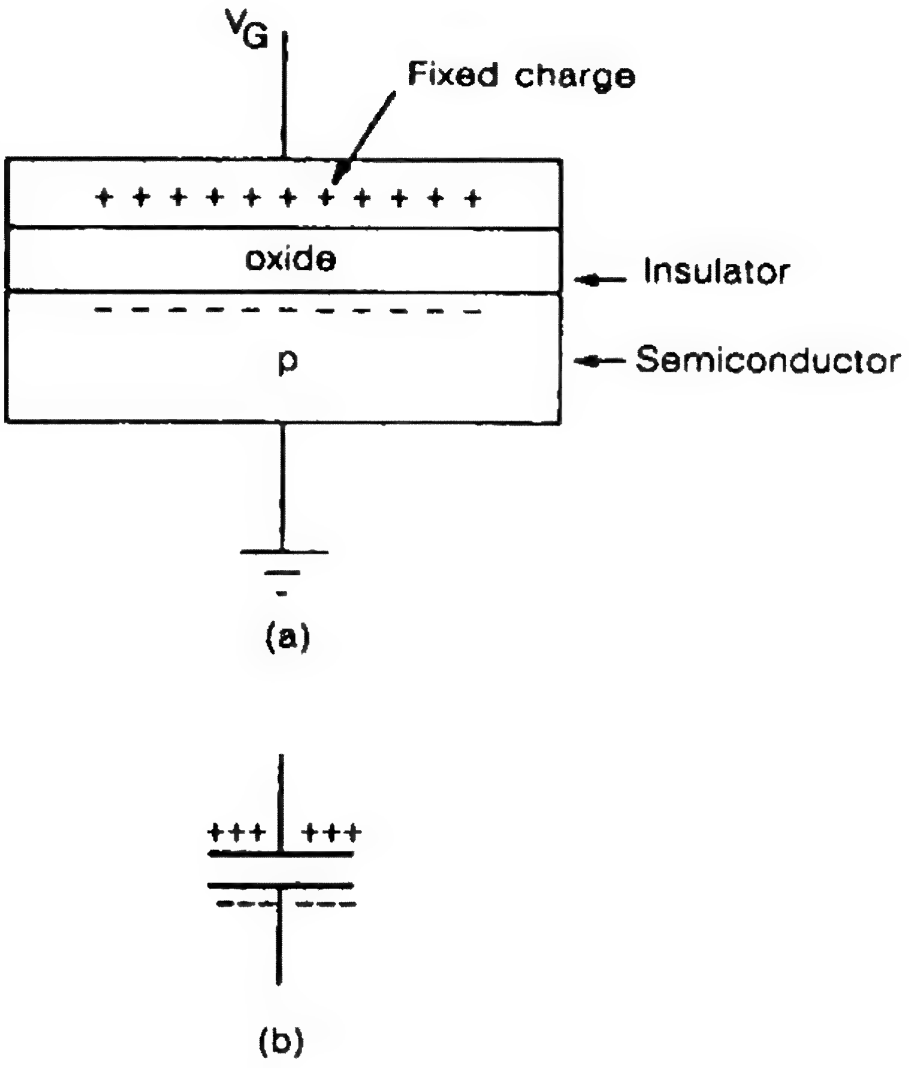


Figure 1.7 The MOS capacitor consists of the gate electrode, the oxide (insulator), and the semiconductor (a). The electrical analog is the simple capacitor. Note that equal and opposite charges rest on the two plates (b).

1.3.2 The Analogy to the MOSFET

One plate of our capacitor is the MOSFET gate, the silicon dioxide being the dielectric and the opposing "plate" the doped silicon of the FET itself. Figure 1.8 provides a rudimentary cross-section of an n-channel, enhancement-mode MOSFET. In this view we have a p-doped silicon substrate into which have been diffused two n-doped wells. The n^+ merely suggests a more heavily doped semiconductor than n (which, in turn, is more heavily doped than n^-).

A positive charge on the gate will attract the electrons resident in the p-substrate to accumulate beneath the gate oxide.

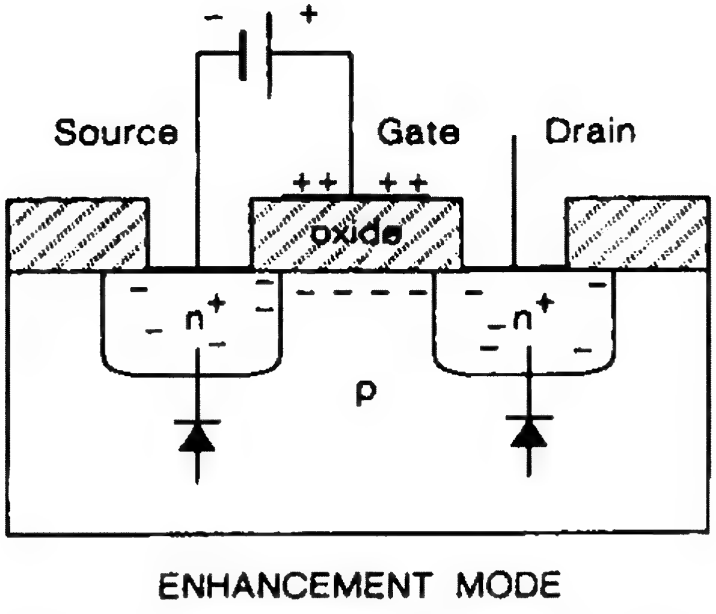


Figure 1.8 The basic enhancement-mode MOSFET with a positive gate-source bias to effect what is called inversion. As the gate potential rises, more electrons will be attracted beneath the gate oxide, and a conducting channel will bridge from source to drain.

The amount of charge, reflected as a potential, on the gate will control the density of the accumulated electrons.

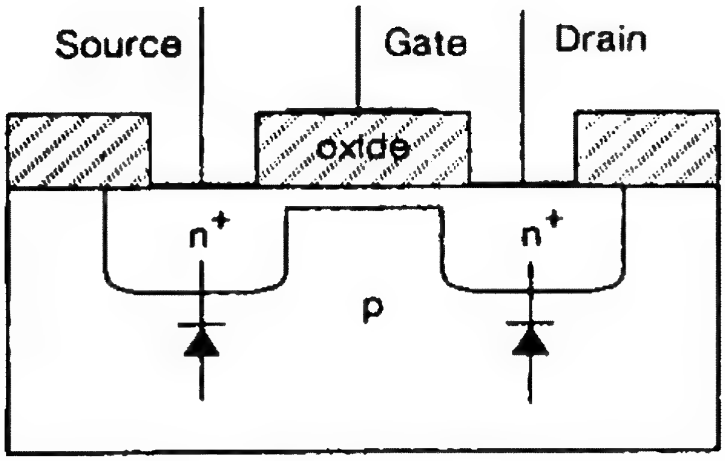
The accumulation of electrons acts like an n-type surface layer superimposed on a p-doped substrate. What we have, as a result of the accumulation of (n) electrons, is now called *inversion*. That is, what was formerly p (hole) dominant is now n (electron) dominant.

At this point we witness a continuous n-path extending from source to drain. Current is free to pass between the terminals.

The depletion-mode MOSFET, shown in Figure 1.9, differs from the enhancement-mode MOSFET by the addition of a conducting channel spanning from the source diffusion to the drain diffusion allowing for the free flow of current.

Remembering that this mode of FET operates with a gate voltage whose polarity opposes that of the drain, we place a negative voltage on the gate. As we build up a negative potential on the gate, positive charges accumulate within the channel beneath the gate oxide, and a depletion region spreads across the channel, cutting off the flow of current.

However, there is one unique aspect of the depletion-mode MOSFET. If we reverse the polarity of the gate potential, changing to positive what we show in this example of an n-channel MOSFET as negative, rather than accumulate positive charges



DEPLETION MODE

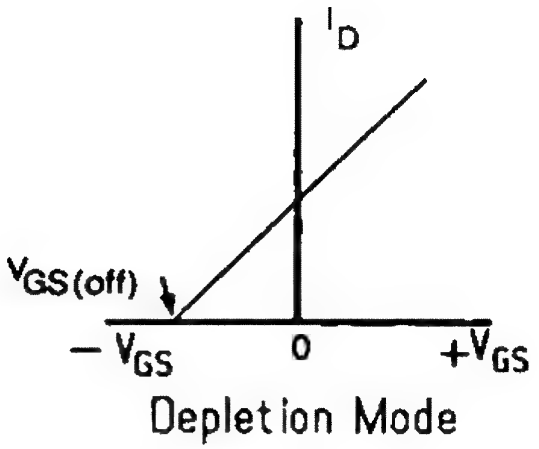
Figure 1.9 The depletion-mode MOSFET contains a conducting channel when no gate bias is applied. Operation of this style closely follows that of the JFET, where a reverse-biased gate voltage depletes the channel.

beneath the gate oxide, we will further enhance the n-doped channel. The result is that our depletion-mode MOSFET may also operate as an enhancement-mode MOSFET! Figure 1.10 offers the transfer characteristics of both the depletion-mode and enhancement-mode MOSFETs. That we cannot reverse the performance of the enhancement-mode MOSFET—to take on depletion-mode characteristics—should be clear as we study Figure 1.10.

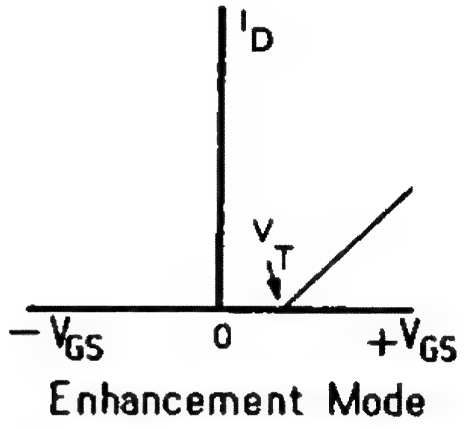
The MOSFET we have just described, developed both as an n-type as well as a p-type, made possible the opportunity for monolithic complementary pairs, called CMOS (complementary metal-oxide-semiconductor).

1.4 Small-Signal, Double-Diffused MOSFETs (DMOSFETs)

Although the MOSFET was a major step in the evolution of majority-carrier transistors, the present design, understandably, did not offer the performance that had been predicted. The shortcoming that prevented this hoped-for performance was the size of the channel beneath the gate. Because of basic limitations in production-oriented photolithographic techniques (masking), a channel approximately 7.5 micrometers wide and 5 micrometers long was about the limit. To achieve both faster switch-



(a)



(b)

Figure 1.10 Transfer characteristics of the depletion-mode (a) and enhancement-mode (b) MOSFETs.

ing and higher frequency response, as had been earlier predicted, the channel length would have to be reduced to close to 1 micrometer.

1.4.1 Physical Differences of DMOS

The solution to achieving short channel lengths was found to be possible by a double diffusion within the same masking operation. For an n-channel DMOS, the first step was the diffusion of p-type material into which was then diffused an n-type dopant. Figure 1.11a provides a rudimentary cross-section of these two

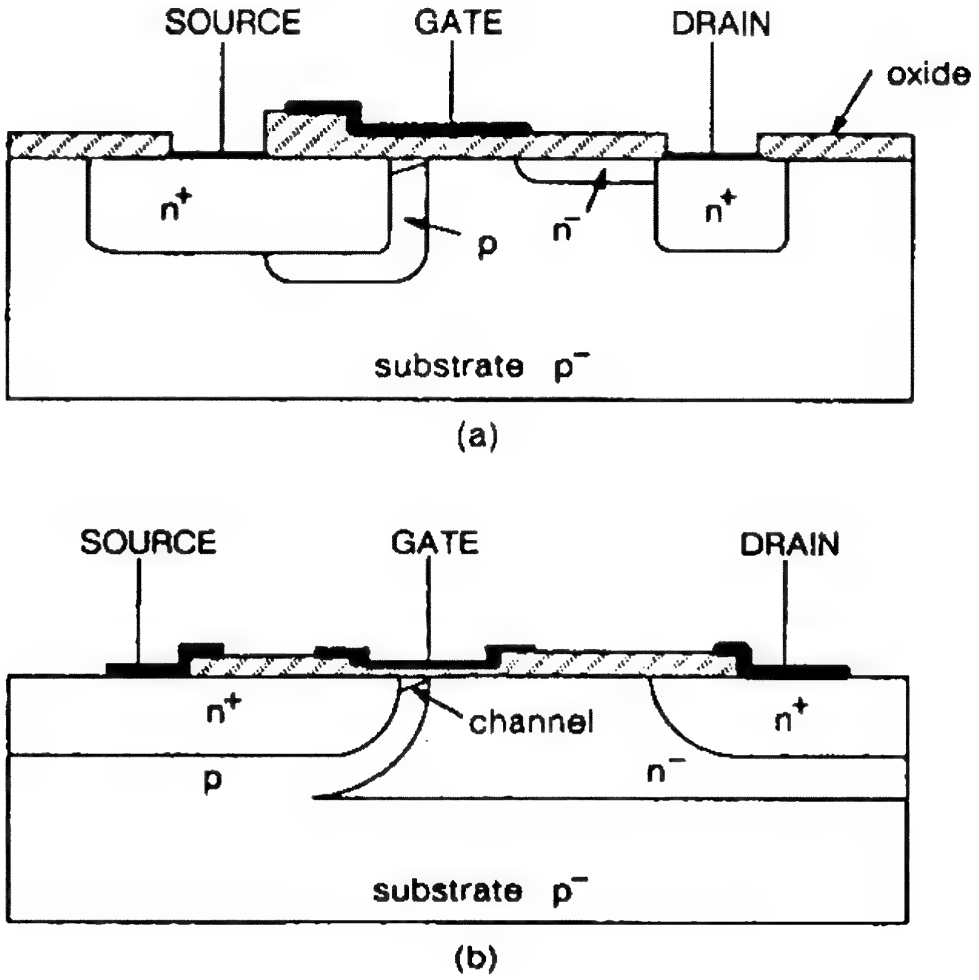
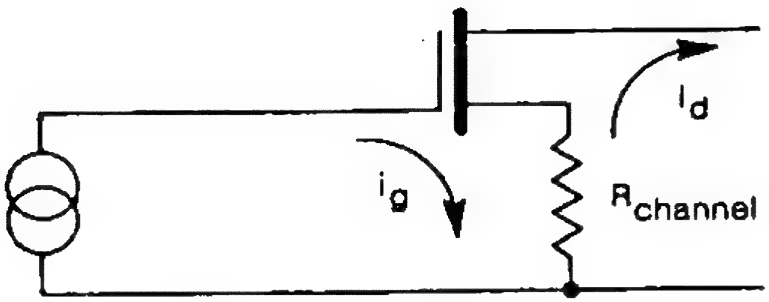


Figure 1.11 A rudimentary cross-sectional view of the small-signal, double-diffused MOSFET, showing two manufacturing procedures. (a) The p^- channel is diffused first, followed by the diffusion of both the source and drain (n^+) diffusions. (b) A deep n^- diffusion into the p^- epitaxy is followed by both source and drain (n^+) diffusions. Most manufacturers follow the first procedure.

subsequent diffusions with a single mask. By careful control of the dopants used for both the p and n diffusions as well as of the time and temperature used in the processing, we are able to achieve precise channel lengths as short as a micrometer!

An alternate method would be to first grow an n^- epitaxy on a p-doped wafer and, when diffusing the p-type material, have it penetrate through the epitaxy into the p-substrate. Then proceed as before with the second diffusion (of n-type dopant) into the existing p-doped well. This is shown in Figure 1.11b.

The short channel provided additional benefits, itemized below:



EQUIVALENT CIRCUIT showing degeneration path

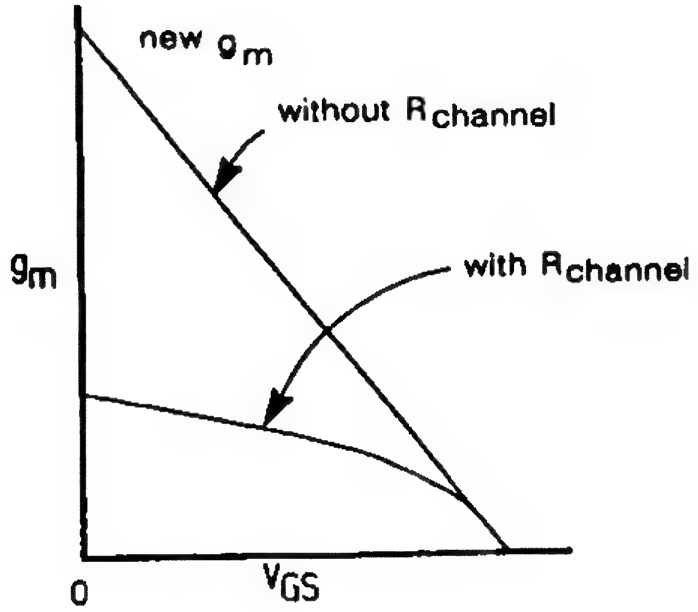


Figure 1.12 An equivalent circuit showing how channel resistanc contributes to degeneration, accompanied by plot of g_m (forward transconductance: see Section 3.3.4) versus V_{GS} (gate-source voltage).

1. Greatly diminished degeneration (see Figure 1.12)
2. Improved forward transconductance
3. Reduced ON-resistance
4. Reduced parasitic capacitances

There were two additional shortcomings of the basic MOSFET design that we were able to overcome using the DMOS technology These were:

1. A too-low avalanche breakdown between drain and source/gate
2. Punchthrough of the drain-depletion region to the source (see Figure 1.13)

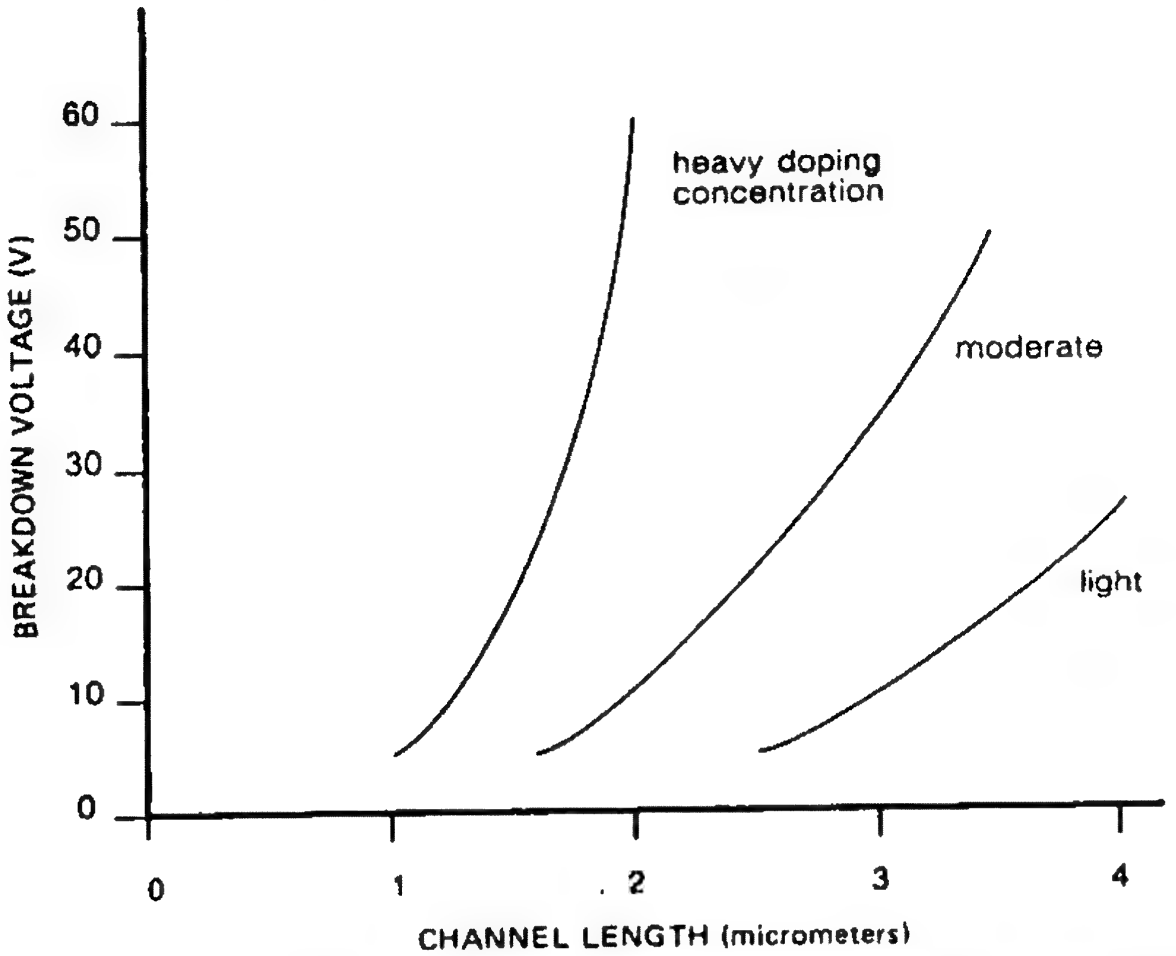


Figure 1.13 The breakdown phenomenon known as "punchthrough" is greatly affected by the epitaxy doping concentration.

To overcome these two shortcomings, a lightly doped n^--region extends from the n^+-doped drain diffusion out to the p-doped channel. This n^- "drift region," although allowing for higher drain potentials, does contribute to an effect known as transit time, which may limit high-frequency performance.

The early production DMOSFETs were fabricated using a deposited metal gate. Later some manufacturers replaced the metal gate with a polysilicon gate, which was believed to offer greater stability and reliability but at the expense of performance at ultrahigh frequencies.

1.5 Large-Signal, Static-Induction Transistors

There were fundamental problems associated with the small-signal JFET that made it nearly impossible to control heavy currents or

high voltages. Certainly the classic planar JFET appeared destined to remain a low-power transistor, despite many vain attempts to resolve the problem. Simply by increasing the size of the geometry to achieve greater current-handling ability was destined to failure, for as size increased, the ratio of transconductance to capacitance decreased. As a consequence, the figure of merit plummeted. In a successful design, the ratio would have to increase. That is, we would wish for an increased figure of merit. An additional and far more serious problem was that as the semiconductor chip grew in size to accommodate the increased current, the yield (the number of electrically good dies per wafer) dropped.

1.5.1 Physical Comparison to the JFET

A dramatic change in the philosophy of FET design occurred when Wegener proposed a cylindrical JFET based on Poisson's equations that showed a marked improvement in the saturation drain current at low pinch-off voltages. The comparison shown in Figure 1.14 between the classical and the cylindrical JFET is

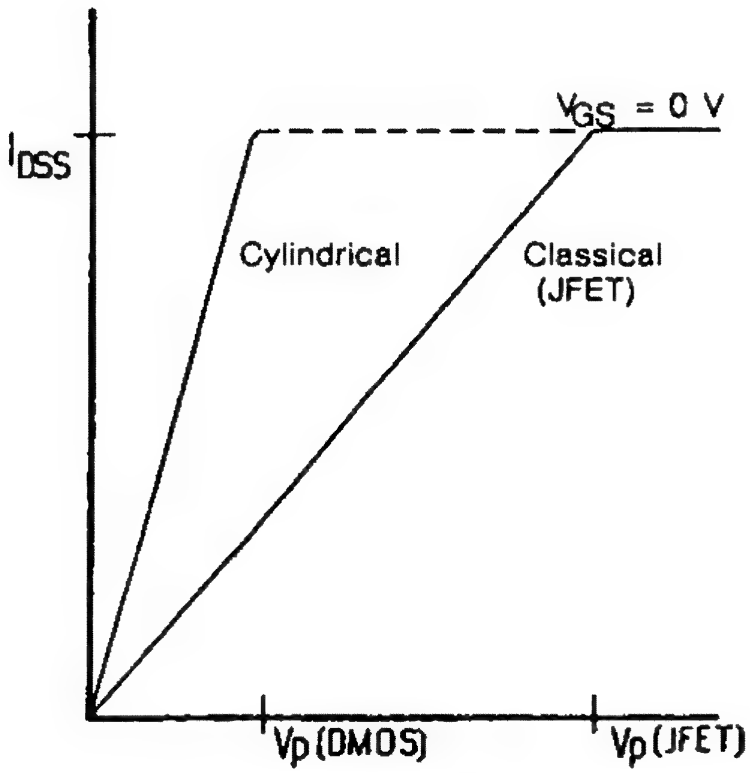


Figure 1.14 Comparison of the performance of the classic JFET with that of the cylindrical JFET propsed by Wegener. Note the dramatic improvement (lowering) of V_p and $r_{DS(on)}$ [slope] for the cylindrical JFET.

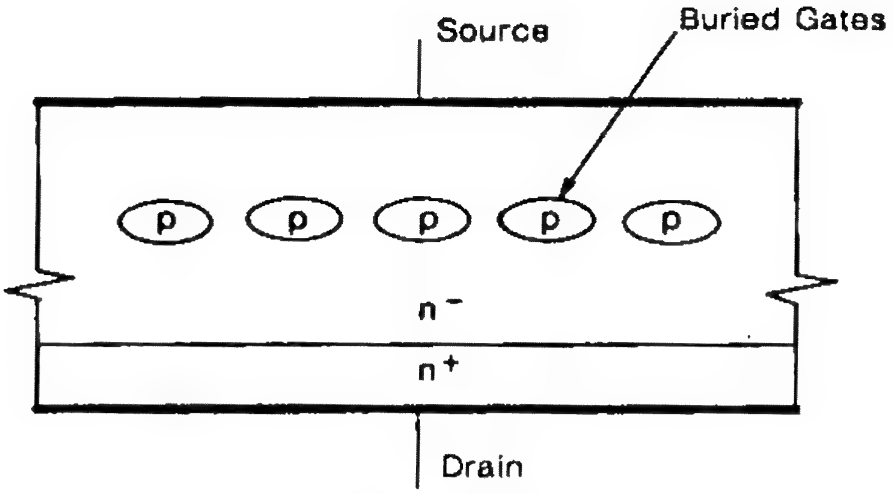


Figure 1.15 Zuleeg's "MUCHFET" (multichannel FET). Note that the drain is on the underside of the chip.

striking. Soon after, both Teszner and Zuleeg offered designs of what became known as the analog transistor, using the cylindrical concept. This transistor was a JFET that could handle high currents. A simplified cross-sectional view was offered in Figure 1.15.

Shortly thereafter, Nishizawa introduced the static-induction transistor (SIT) shown in Figure 1.16, which is indistinguishable from the analog device shown in Figure 1.15.

There are at least three principal advantages of both the analog and static-induction transistors. These are:

1. The extremely high channel conductance, which greatly diminished the degeneration effect—the Achilles' heel of the classic small-signal JFET (refer to Figure 1.12)
2. The capability of withstanding high voltages
3. The ability to operate at very high frequencies, possibly into the microwave region

1.6 Large-Signal (Power) MOSFETs

Although the small-signal DMOSFET that evolved was far superior to the earlier MOS design, nonetheless it was unable to support the very high voltages that are expected in heavy industrial applications. Additionally, if heavy currents were to be controlled, a more efficient topology was mandatory, if for no other reason than to maintain a reasonable chip size with useful yields.

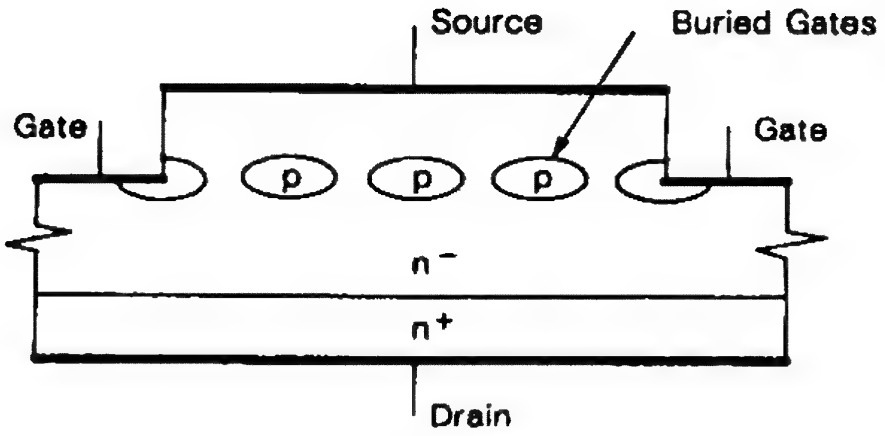


Figure 1.16 Nishizawa's static-induction transistor. Note the similarity to Zuleeg's MUCHFET (Figure 1.15).

We could not afford a top drain contact on the surface of the semiconductor die.

1.6.1 Physical Differences of Power MOSFETs

Hitachi of Japan introduced the first *vertical* power MOSFET in 1969, but it was not until Ragle perfected the concept at Siliconix in 1976 that the power MOSFET became practical for commercial use. A major deviation from the small-signal DMOS concept (Figure 1.11) was the placing of the drain terminal on the under side of the semiconductor. Throughout this book we refer to the vertical power MOSFET using the acronym DMOSFET.

1.6.2 The V-Groove MOSFET

However, the early power MOSFETs that were developed by Ragle in the United States differed dramatically from those in general use today. Rather than having a polysilicon gate located laterally on the surface of the structure, a V-groove was anisotropically etched through the double diffusion (power MOSFETs, whether V-groove or planar *are* DMOS). An oxide layer was grown across the surface and into the V-groove, and aluminum was carefully deposited with the aid of masks, to provide a source contact as well as a gate. A detailed cross-section is shown in Figure 1.17a. Unfortunately, the sharp radius of curvature of the V-groove resulted in premature breakdown. To offset this, the truncated V-groove (Figure 1.17b) evolved.

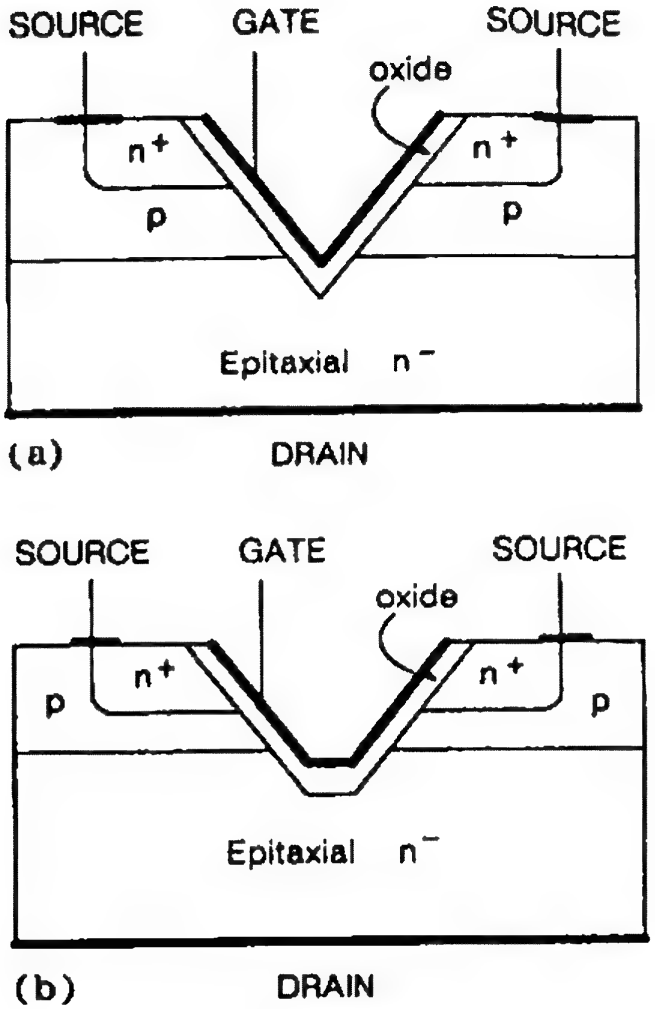


Figure 1.17 (a) Cross-sectional view of the first commercially available power DMOSFET. Note the sharp V-groove, which was later found to limit the breakdown voltage. The VMOSFET is a vertical structure with drain on the underside of the chip. The parasitic npn bipolar transistor is muted by source metal bridging from the n^+ (the pseudo-emitter) to the p (the pseudo-base). (b) Cross-section of the truncated VMOSFET, where the flat bottom offered a much-improved high-voltage capability. Despite the advantages in high-frequency performance, the problems encountered in manufacture soon discouraged its use for low-frequency power applications. Note the similar n^+-to-p bridge to mute the parasitic npn bipolar transistor.

1.6.3 The Lateral Geometry Power DMOSFET

When the Japanese introduced their commercial product, much of the world was surprised to discover that it was incompatible with the power DMOSFETs available elsewhere. The pin-out of the package was different. Why?

Whereas most power DMOSFETs were fabricated with the drain contact on the underside of the semiconductor chip, the Japanese fabricated their devices with the drain contact on the surface of the semiconductor. This resulted in one favorable attribute: it allowed packaging of the transistor in the classic TO-3 metal can with the case at ground potential. Other than this singular advantage, the fact that no second source was available limited the sale of the Japanese DMOSFETs. Among the faults of this design concept was the inability to produce dense geometries capable of withstanding high currents and high standoff voltages.

1.6.4 The Vertical Geometry

The modern-day power DMOSFET still sports a vertical concept in that the drain remains beneath the semiconductor (the Japanese are now offering a similar product). However, the evolutionary process since the original V-groove power MOSFET has brought about some radical changes, not only in the cross-section but in topology as well. Figure 1.18 offers a typical cross-sectional view of today's power DMOSFET. Although manufacturers tend to choose their own topologies, there have been published studies comparing geometries for optimum performance. The results of one such study are shown in Figure 1.19.

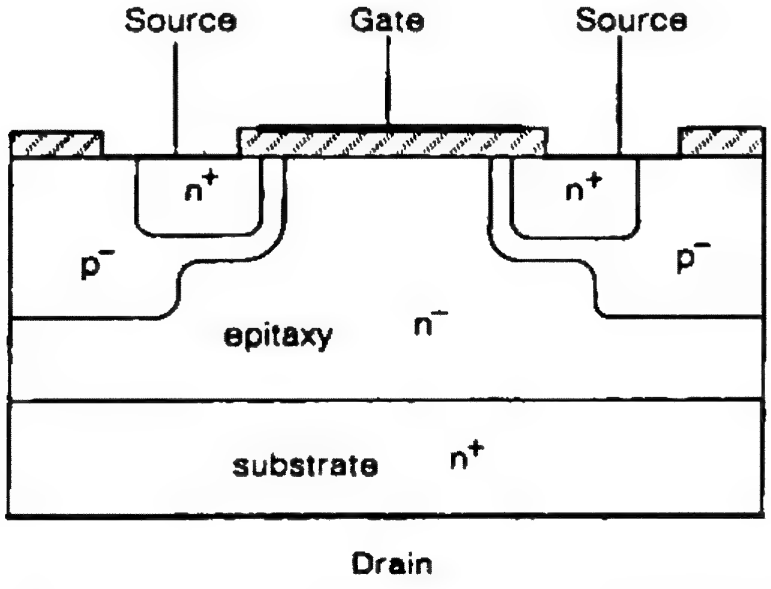


Figure 1.18 A cross-sectional view of today's modern n-channel enhancement-mode power MOSFET. Note the similar means whereby the parasitic bipolar device is muted with a bridge across source to body.

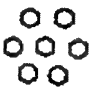
Square on Square Grid	Circle on Square Grid	Hexagon on Square Grid	Square on Hexagon Grid	Circle on Hexagon Grid	Hexagon on Hexagon Grid
					
					
1.0	.886	.931	1.07	.952	1.0

Figure 1.19 The many topologies that are used by various vendors of power MOSFETs.

1.7 Large-Signal, Insulated-Gate Bipolar Transistors

The power DMOSFET was not a panacea for heavy industry. To date (1987) it has proved impractical for high-voltage, high-current application, where both features were needed simultaneously.

In the early 1980s General Electric introduced the "IGT"—the insulated-gate transistor—an unusual power transistor exhibiting a MOSFET input and a bipolar transistor output. [General Electric, and the industry at large, has renamed the device the "insulated-gate bipolar transistor," which more closely identifies its operation. In this text we will use the corresponding acronym: IGBT.]

1.7.1 Physical Differences Between the IGBT and the MOSFET

A cross-sectional view of an IGBT is presented in Figure 1.20. Several advantages were achieved by this novel cascade construction, not the least of which is the tremendous increase in current-handling capacity (shown in Figure 1.21). The greatest boost the IGBT offers is the capability to control massive power levels, greater even than those possible with a bipolar junction transistor, in voltage as well as simultaneously in current, with

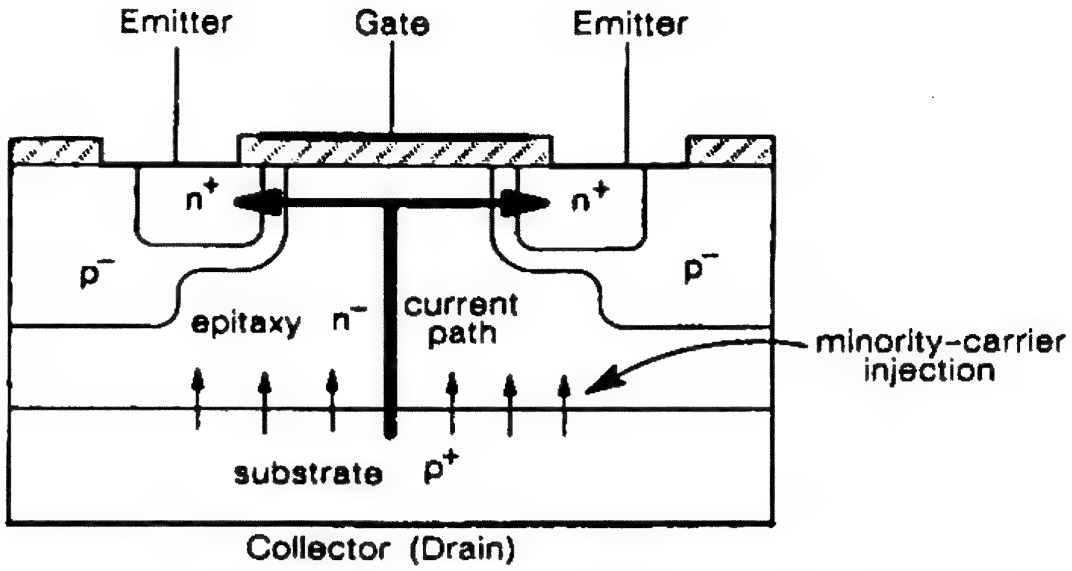


Figure 1.20 The insulated-gate bipolar transistor looks very much like the power MOSFET, but take a careful look at the substrate! Unlike DMOS, the IGBT has another pn junction (substrate-epitaxy).

the ease popularized by the power MOSFET—through a high-impedance gate electrode.

Applications needing the high-voltage, high-power capabilities of the IGBT must contend with its bipolar turn-OFF characteristics. Attempting faster turn-OFF by manipulating the gate may lead to a catastrophic SCR-type latch-up condition.

Yet, many profess that quite possibly the only real benefit afforded by the IGBT is to provide a less expensive power transistor than the comparable power DMOSFET—if, indeed, a power DMOSFET of comparable capacity can be built.

To allay any hopes that the IGBT might supersede the power DMOSFET at low voltages, we need only recognize the p-n interface within the substrate/epitaxy, which, at best, forces a diode drop at *any* current. Consequently, as the current rises, this diode drop contributes to increasing the apparent $r_{DS(on)}$ of the IGBT. The net effect results in a dramatic increase in the saturation voltage $V_{CE(sat)}$. At competitive voltages, power DMOSFETs, with their lower saturation voltage $V_{DS(on)}$ can easily outperform the IGBT both in current and in power.

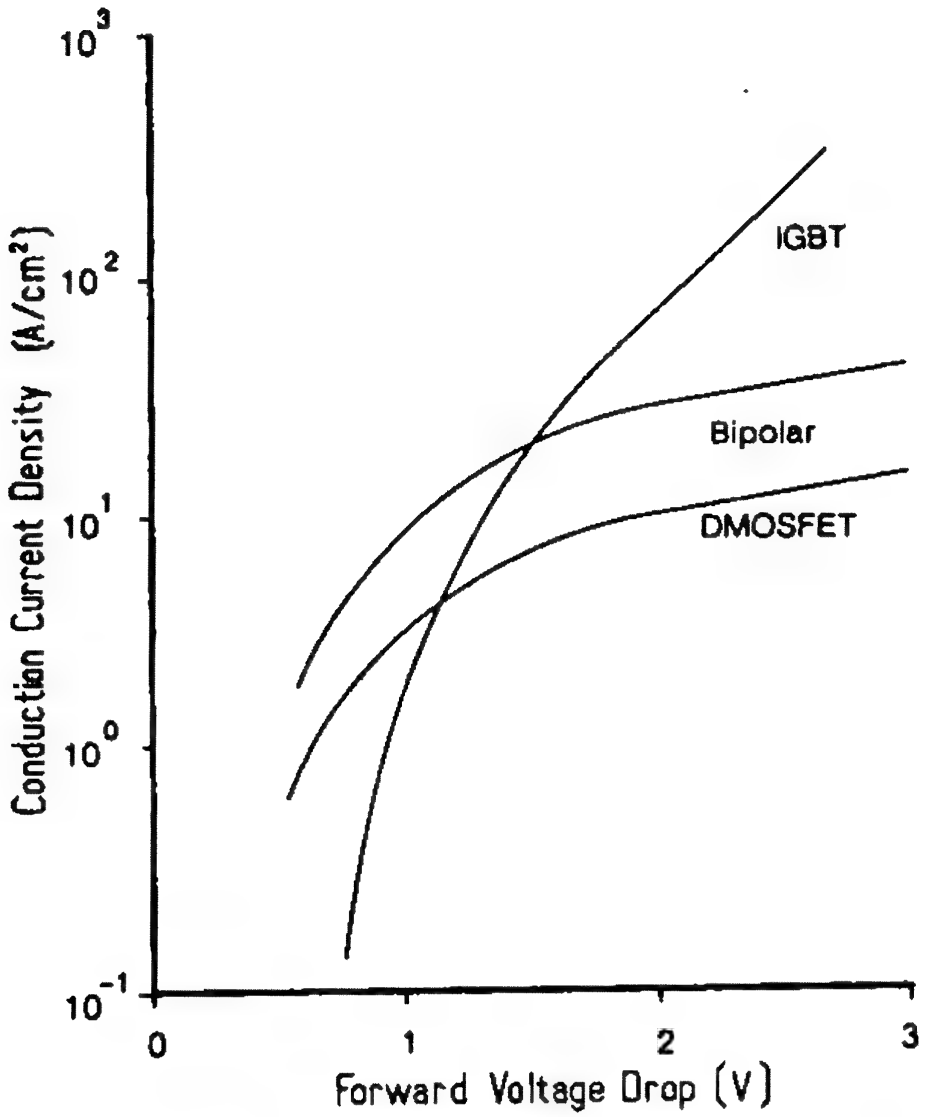


Figure 1.21 Comparison of the relative current capability of an equal area geometry bipolar transistor, a power DMOSFET, and the IGBT. Note that the IGBT shows a distinct advantage only at higher currents; the disadvantage lies in the higher forward voltage drop (saturation voltage) at low conduction current densities.

1.8 Other MOS-Gated Structures

Thyristors that can be turned ON as well as OFF by the application of a gate drive are called "gate turn-OFF thyristors," or GTOs. Operationally, they differ radically from FETs; consequently they are not discussed in this book. They are not majority-carrier transistors as are JFETs and MOSFETs, nor do they operate like the IGBT (that is, ON like a FET, OFF like a bipolar transistor).

A new product that at the time of this writing has not received wide acclaim is the MOS-gated GTO. This structure, however, suffers in that, generally, it requires *two* gates: one to turn ON, the other to turn the GTO OFF. A newer product currently in development is the MOS-controlled thyristor, or MCT. Whereas the IGBT appears to offer superior performance (compared to the power DMOSFET), ranging from 500 to 1200 V at currents upward of 50 A, the MCT, hopefully, will encourage performance beyond 1200 V and 50 A.

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2

How They Work

In a Layman's Language

2.1 Introduction

We devote this chapter to an in-depth study of how each of the devices works. Although in Chapter 1 we touched on the performance mechanics of gated structures of different types, our intent was to identify structural differences rather than to concentrate on the details of operation, as we do in this chapter. In keeping with our original intent to make this text understandable to a wide readership, we continue to describe the details of operation phenomenologically, in other words, in a manner that offers an intuitive sense of how they work. We assume the reader to have some understanding of semiconductor physics as well as electronic circuits. References given at the conclusion of this chapter, as with other chapters, guide the reader to literature that offers a more technical description of how different gated structures work.

FETs are *field-effect* transistors; as the generic name implies, they operate on the principle of the electrical manipulation of fields. In all cases this field manipulation is under the control of the gate, which, in turn, acts on the conduction of carriers in a semiconductor channel. Furthermore, because they do not operate on the principle of minority-carrier injection, as does the bipolar transistor, FETs are noted as being majority-carrier transistors.

2.2 Small-Signal JFETs

We add to our intuitive understanding of JFET operation by imagining a bar of n-doped semiconductor placed in a current loop. That is, having an impressed voltage across the terminals of the semiconductor, a current flows whose magnitude depends on such factors as this impressed voltage and the resistance of the semiconductor. The latter depends, among other things, on the doping concentration, the length, and the cross-sectional area of the semiconductor.

As users of this JFET, we generally have the option to modify the applied voltage but certainly we cannot opt to change either the dopant, its concentration, or the physical construction of the semiconductor. To control this current flow we have but two options: alter the applied voltage, or alter the channel resistance. The former, although certainly possible, is generally neither practical, nor desirable, leaving alteration of the channel resistance as our only option.

The gate terminal remains our only viable control. What we wish of the JFET we must obtain by the manipulation of gate bias. The effective control of channel current demands control over the depletion fields within the channel. This we learned in Chapter 1.

Our concept of depletion, as gained from Chapter 1, is incomplete because we did not consider the contribution of the drain potential. Heretofore, we presumed the drain potential to be 0 V; but seldom do we operate a JFET with near-zero drain voltages, except possibly as a voltage-controlled resistor (VCR).

A more complete understanding of how applied voltages affect the depletion regions is offered in Figure 2.1. In Chapter 1 we learned how the gate-to-source voltage affects the depletion regions. Here, we identify the effect of the drain-to-source voltage V_{DS}. As we initiate an increased V_{DS}, two events occur:

1. The drain current increases.
2. The space-charge width (depletion region) in close proximity to the drain terminal expands, decreasing the channel conductance.

As we continue increasing V_{DS}, the channel conductance continues to decrease until the drain current reaches a state of equilibrium at which, with further increases in drain voltage, we see no increase in drain current. This point of equilibrium, or

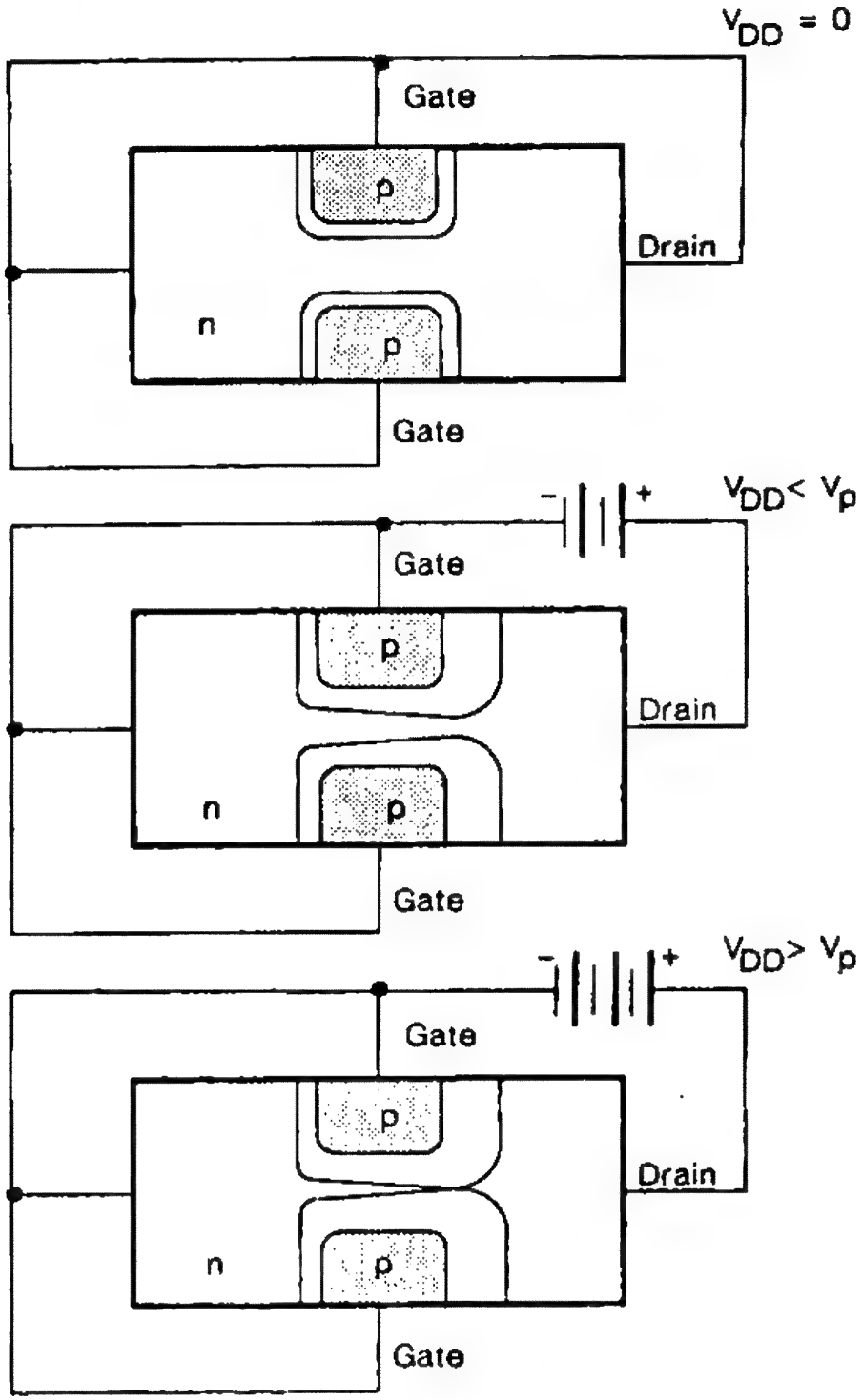

Figure 2.1 Channel depletion versus drain-source voltage.

saturation, is termed the *drain saturation current*, I_{DSS}, and the drain-source voltage at which it occurs is called the *pinch-off voltage*, V_p.

If the channel is long compared to its width, the absolute value of V_p is approximately equal to the absolute value of the gate cutoff voltage $V_{GS(off)}$, or,

$$|V_p| = |V_{GS(off)}| \tag{2.1}$$

Should the channel be short compared to either its width or its thickness, the absolute value of V_p may differ from the gate cutoff voltage by as much as 1.6 times!

These short-channel FETs experience an effect known as *velocity saturation*. This phenomenon is more fully explained in Section 2.4. A common misconception is that *all* FETs operating in their saturation region are in velocity saturation.

The concept of "pinch-off" tends to be confusing since, in actual operation, the channel current is *not* pinched off. Channel current is truly pinched off only when the drain current is zero. Under the conditions described here, this is not the case. Here the channel current remains finite, hence at V_p we have remaining a thin conducting region consisting of a very high current density and an intense electric field.

As the JFET approaches the condition of drain-current saturation two events occur.

1. As V_{DS} rises, the drain current also rises rapidly, for in this pre-pinch-off region the JFET is considered to be operating in its triode state.
2. As V_{DS} rises, the depletion region in proximity to the drain enlarges, which, in turn, decreases the incremental channel conductance.

Not until we pass pinch-off does the conductance tend to reach its lowest value. Were we to examine the output characteristics, we would generate a series of curves similar to those shown in Figure 2.2.

Careful study of Figure 2.2 identifies a special relationship between V_{GS} and I_D. As the gate becomes more negative, with respect to the source, the saturated drain current I_D decreases and the value of V_p also decreases by the approximate magnitude of V_{GS}!

To obtain a better understanding of FET operation, we need to examine Shockley's equation, which describes the operation of the simple long-channel JFET:

$$I_D = I_{DSS}\left[1 - \left(\frac{V_{GS}}{V_{GS(off)}}\right)\right]^n \qquad (2.2)$$

This equation shows that when our gate bias V_{GS}, is equal to $V_{GS(off)}$, the drain current I_D is zero. On the other hand when V_{GS} is zero (0 V), I_D is equal to the saturation drain current I_{DSS}.

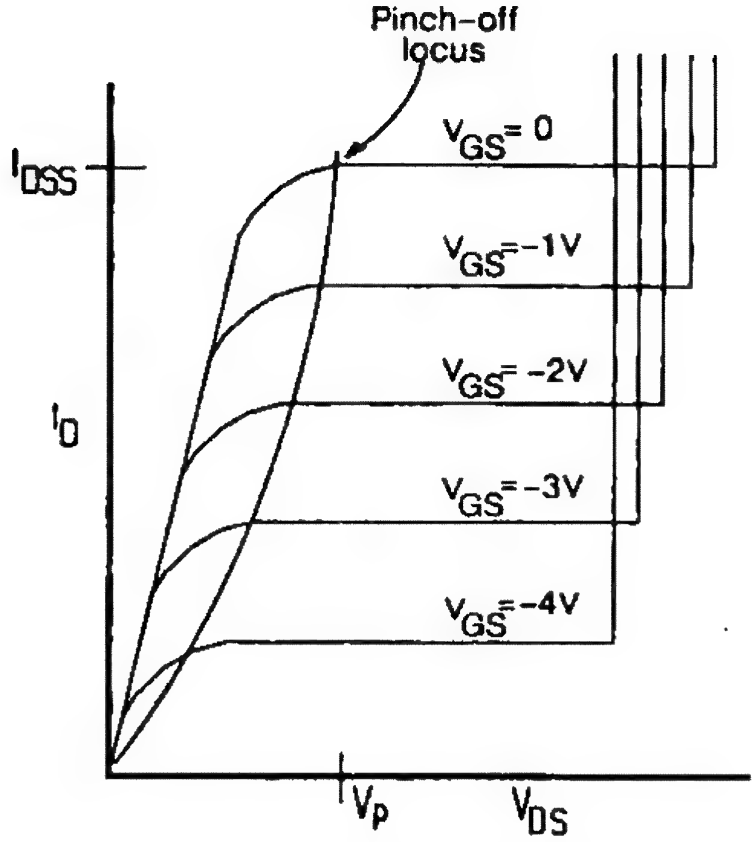

Figure 2.2 Output characteristics of a depletion-mode, n-channel FET. Pinch-off locus of V_{DS} identifies where I_D saturates at each bias level.

2.3 Small-Signal MOSFETs

As we learned in Chapter 1, the MOSFET differs from the JFET in that the former may be operated in the *enhancement* mode as well as in the *depletion* mode. Furthermore, we saw that MOSFETs can be constructed solely as enhancement-mode devices. Unlike the JFET, the gate can accept potentials of either polarity, generally without harm to the device. We should take note, however, of two potential constraints.

1. The oxide becomes the gate insulator, which limits the magnitude of gate voltage. Should a rupture occur, caused by excessive gate voltage exceeding the dielectric breakdown of the gate oxide (for SiO_2, approximately 6×10^6 V/cm), the gate structure and thus the MOSFET are invariably destroyed.
2. Small-signal MOSFETs exhibit low input, or gate, capacitances. To ensure the safety of the gate, some MOSFETs have zener diode clamps to thwart any static potentials from building on the high-impedance gate structure.

Consequently, gate voltage constrains often exist for most small-signal MOSFETs.

Aside from the basic operational differences in gate control, the single-gate MOSFET, unlike the three-terminal JFET, is a four-terminal device. The fourth terminal—the substrate—is often shorted to the source.

2.3.1 The Depletion-Mode MOSFET

Operating similarly to the JFET, the depletion-mode MOSFET likewise exhibits a drain-current saturation characteristic but with a notable difference. The drain saturation current I_{DSS}, can be exceeded by "forward" biasing the gate. Whereas with the JFET this results in forward gate-diode conduction, with the depletion-mode, insulated-gate MOSFET, operation slips into the enhancement mode. Figure 2.3 is a classic illustration of this dual role for the small-signal, depletion-mode MOSFET. The limit of enhancement depends solely on the dissipation of the package. If the gate is zener-protected, however, forward biasing may not be possible, thus limiting enhancement.

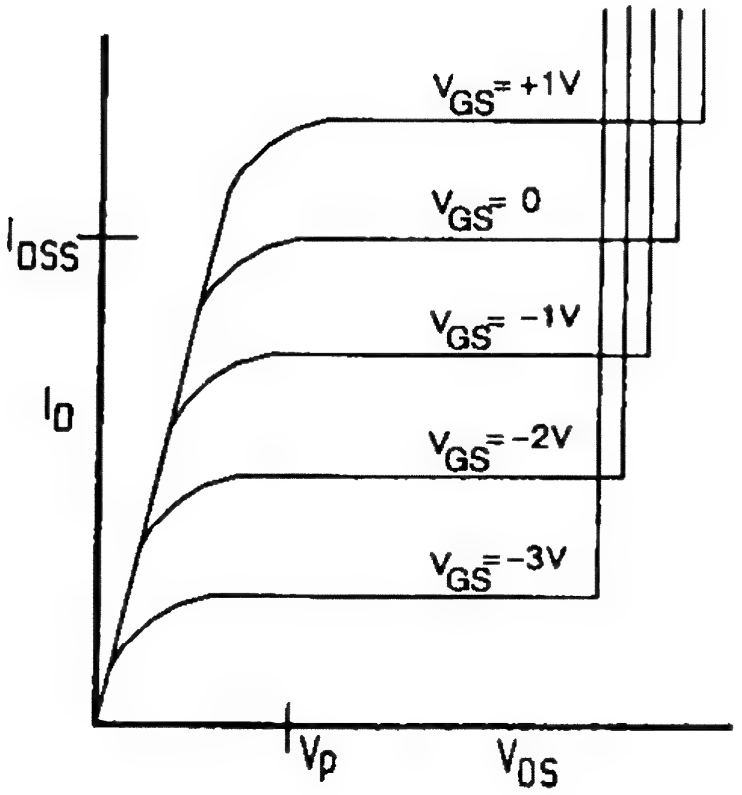

Figure 2.3 Output characteristics of a depletion-mode, n-channel MOSFET "enhanced" by the application of positive gate bias.

Because we are able to bias a depletion-mode MOSFET to perform like an enhancement-mode MOSFET, we are again reminded of how like and unlike charges behave. A depletion-mode MOSFET, shown earlier in Figure 1.9, possesses a channel spanning between source and drain. When a positive potential is impressed upon the gate, a corresponding charge of electrons is attracted to the channel causing (in the p-doped substrate) an inversion layer immediately adjacent to the diffused channel. In combination with the existing channel, this inversion layer bridges across from source to drain, contributing to raising the conduction properties of the MOSFET. Figure 2.4 is a simplified schematic diagram portraying these events.

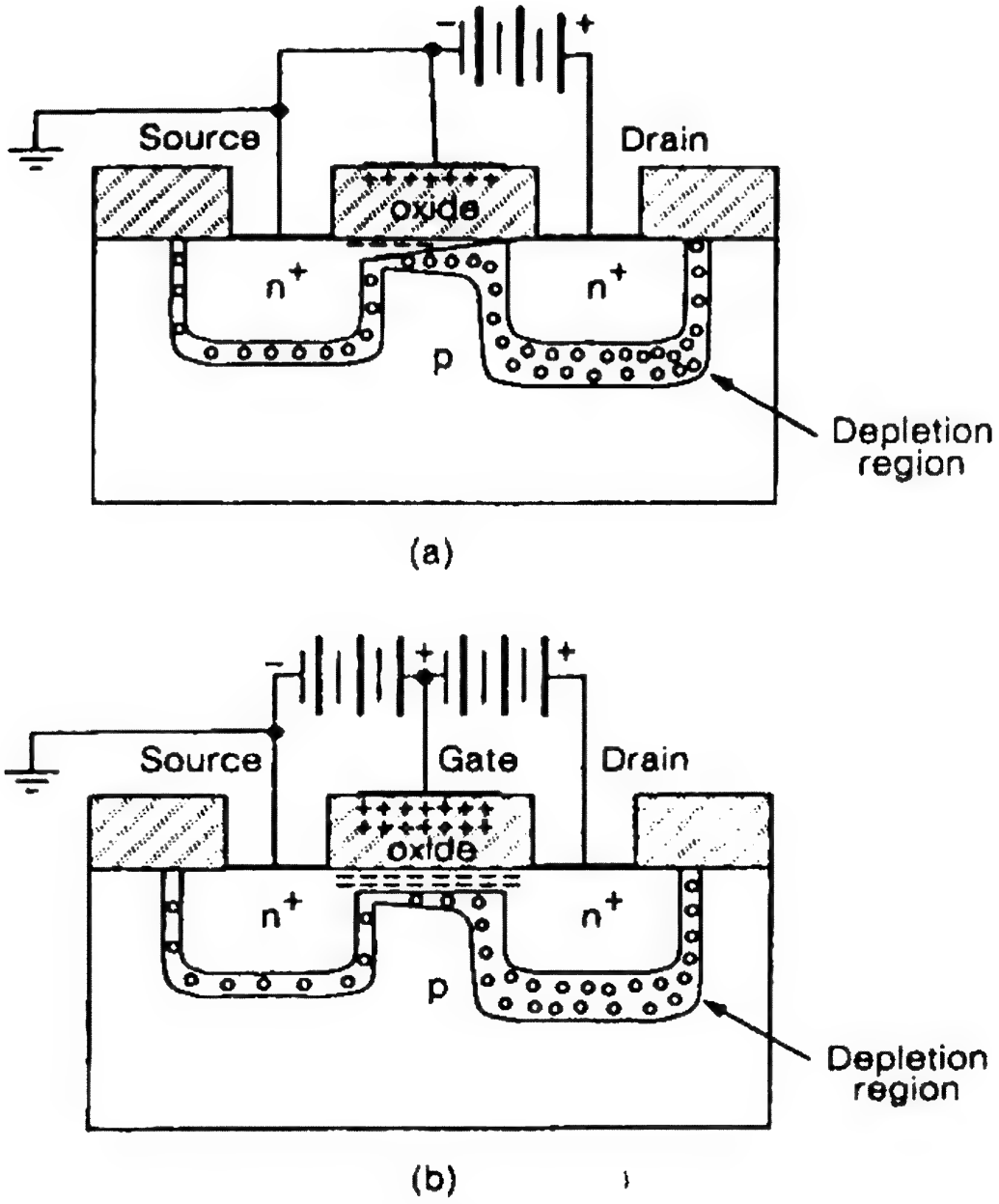

Figure 2.4 (a) Depletion region of a depletion-mode, n-channel MOSFET with zero gate bias. (b) Enhanced channel of same MOSFET with gate forward biased.

Within the family of small-signal, depletion-mode MOSFETs, if we examine what is commonly used in many ultra-high-frequency receivers, notably TV, we find the familiar dual-gate MOSFET. This MOSFET is essentially a monolithic pair of MOSFETs in cascade. The principal advantage of this cascade-connected pair is that it provides a tenfold increase in the gain-bandwidth product, because of the similar tenfold decrease in feedback capacitance.

This reduction of feedback capacitance results from the heavy loading, by virtue of the low r_{DS} of the second MOSFET, of the first (MOSFET) stage of amplification in combination with the RF-grounded gate of the second MOSFET.

2.3.2 The Enhancement-Mode MOSFET

The enhancement-mode MOSFET is normally OFF when no gate potential exists and will turn ON only when the polarity of the gate voltage matches that of the drain voltage. The concentration of induced carriers, and therefore the conduction of the channel depends on the magnitude of the gate-source voltage V_{GS}, as well as, to a lesser extent, the gate-drain and gate-body voltages.

To ensure a positive gate control to enhance a channel that bridges source to drain, some gate overlap may be utilized. Although overlap is theoretically not necessary for operation, it does allow for the inevitable manufacturing misalignments that occur. Unfortunately, this overlap contributes to increased—and useless—capacitance, both gate-to-source (C_{gs}) and gate-to-drain (C_{gd}). Coupled with the long channel, which contributes to resistance, the overall effect is a MOSFET with poor high-frequency (as well as poor high-speed) characteristics. Modern small-signal MOSFETS often rely on self-alignment masking to eliminate gate overlap.

An enhancement-mode MOSFET requires a finite gate voltage before conduction occurs. The gate voltage at which a somewhat arbitrary level of conduction occurs is called the *threshold voltage*, V_T.

To excite the n-channel MOSFET the gate-source potential is biased positive; for the p-channel MOSFET the gate-source potential is biased negative. At zero gate-source voltage the enhancement-mode MOSFET is OFF, irrespective of whether it is an n- or p-channel device.

What determines the moment of turn-ON (vis., the threshold voltage) is a function of many factors, including the type of gate structure (metal or polysilicon), the thickness and purity of the gate oxide, the doping density of the substrate (or epitaxy) beneath the gate oxide, the body-source voltage V_{BS} (or more correctly labeled, in accordance with JEDEC, the V_{US}: see Section 3.3) and the chip temperature.

The transfer characteristics of both the depletion-mode and the enhancement-mode MOSFET may be reviewed in Figure 1.10.

The careful reader should now be cognizant of the seemingly contradictory definition of the term I_{DSS} for the depletion-mode FET (JFET or MOSFET) and for the enhancement-mode MOSFET. Chapter 3 explains the apparent contradiction.

2.4 Double-Diffused MOSFET (DMOSFET)

The DMOSFET technology has undergone dramatic changes since it was introduced in the mid-1960s. Yet despite notable variations in masking, processing, and application, and aside from physical differences, the small-signal DMOSFET and the large-signal, or power, DMOSFET, have much in common.

2.4.1 The Small-Signal DMOSFET

The small-signal DMOS rose to prominence when efforts were expended to improve the high-frequency performance of the MOSFET. Since the maximum operating frequency depends on the ratio of transconductance to capacity, achieving a higher transconductance and a lower capacitance was the obvious goal. Shrinking the channel length offers both, but, using the conventional MOSFET design constraints, the dual sacrifice of lowered breakdown voltage and increased difficulties in fabrication forced a reexamination of the basic technology. The masking technology had been stretched to its limit to provide such fine definition.

The enhancement-mode DMOSFET performs much the same as the conventional MOSFET as previously described (Section 2.3.2), but with two particular advantages.

1. The channel, being very much shorter, now allows for velocity saturation of the carriers. One aspect of velocity saturation minimizes the effect of gate bias on transconductance, or gain. Consequently, once we have achieved our desired cur-

rent (by means of gate biasing), the transconductance is little affected by further changes in gate bias, allowing for high-speed and/or high-frequency performance at minimum dissipation (power loss).

2. The use of an n-type substrate (or, if the alternate construction is used, as described in Section 1.4.1, n-type epitaxy) provides for the spread of the drain-depletion field into that medium rather than into the channel (as with the classic MOSFET described in Section 2.3), thus offering much higher operating voltages as well as a lower feedback capacitance, C_{gd}.

2.4.2 The Large-Signal (Power) DMOSFET

The large-signal or power DMOSFET needs extraordinarily low channel resistance, $r_{DS(on)}$, to achieve efficient performance at low power dissipation. For seemingly different reasons, the DMOS technology was chosen. Yet even here, to achieve the ultrafast switching speeds a high figure of merit is critically needed. Consequently, we discover that both the small-signal and the large-signal DMOSFETs, indeed, have much in common.

However important a low $r_{DS(on)}$, the short-channel characteristic of DMOS becomes an insignificant contributor! Once we have withholding, or breakdown, voltages much beyond 100 V, the major contributor to the ON resistance becomes the epitaxial drift region. The relationship between the breakdown voltage and the ON resistance of this epitaxy region is:

$$r_{DS(on)} = K\, V_{(BR)DSS}^{2.5} \qquad (2.3)$$

where K is a proportionality constant that also involves the active area of the semiconductor chip.

What we are witnessing from Eq. 2.3 is the effect of the resistivity of the epitaxy. We increase the resistivity to ensure a higher breakdown voltage, but with the increased breakdown capability we also increase the resistance to the current flow. Regrettably, the equation identifies a nonlinear degradation.

Simultaneous with our need for low ON resistance, for the majority of applications in which power MOSFETs are useful, a high withholding voltage is mandated. Since Eq. 2.3 identifies a potentially serious conflict, a struggle ensues in which performance tradeoffs must be balanced against *available* power DMOSFET technology.

Based on Eq. 2.3, a low-ON-resistance, high-breakdown DMOSFET requires a semiconductor chip with a large active area. Early in the development of power DMOSFETs, utilizing the vertical current flow concept—that is, having the drain beneath the chip—was seen as a major benefit. A principal power limitation of the horizontal planar convention, practiced by manufacturers of small-signal FETs and MOSFETs, involved a thin channel. The vertical concept, following that practiced in the manufacture of bipolar transistors, allowed an enormous increase in current handling.

A common practice among manufacturers is to increase the cell density. During the initial phase of power DMOSFET development, when the truncated V-groove was in vogue, cell densities of 20,000 cells per square centimeter were common. During the early 1980s, when the planar DMOS technology superseded the V-groove concept, the density grew to 71,000 cells/cm^2, then to 130,000 cells/cm^2, and today we have densities reaching beyond 250,000 cells/cm^2!

Although such densities offer improved yields of ultra-low-$r_{DS(on)}$ DMOSFETs, we must not overlook the degraded pulse current capability that *may* accompany high-density DMOSFETs. If this degradation exists, it is the result of what is known as the *pinch effect*.

The pinch effect is best understood by examining the cross-section of a power DMOSFET, offered in Figure 2.5.

Electrical contact to the source, gate, and drain uses up potentially valuable active area with lead-bonding pads. Today,

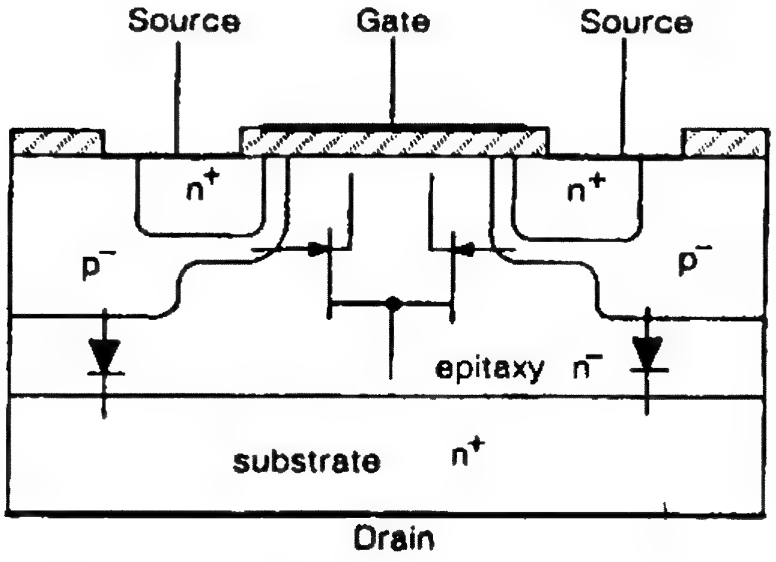

Figure 2.5 The pinch effect results from interaction between the p^- diffusion (acting as a pseudo-JFET gate) and the restricted-area n^- DMOSFET channel.

to achieve even greater utilization of active area, many power DMOSFET manufacturers have removed the source pad and use the technique of "bonding over active area."

The universal practice in the manufacture of power DMOSFETs is to lay source metal over the surface of the semiconductor chip, leaving room, of course, for the gate structure and its lead-bond pad. To "bond over active area" simply means to secure the source lead to this surface metal where it is most convenient. Bonding over active area is a manufacturing option frequently found on super-high-current power DMOSFETs where having a source bonding pad would not lead to efficient utilization of chip area.

Once we have identified our required breakdown voltage, we are faced with two remaining recourses to achieve a higher operating current.

1. Increase the cell density: that is, place a large number of active MOSFETs per unit area in parallel on the chip.
2. Increase the area of the semiconductor chip, which also allows for greater dissipation to the package.

The latter technology is blighted with expensive difficulties, not the least of which is a manufacturing problem involving a statistical concept called "defect density." Many manufacturers have resorted to cleaner production areas to favorably tip the statistics. Figure 2.6 offers a glimpse of how yields are affected by such endeavors.

Operationally, the enhancement-mode power DMOSFET performs exactly as does its small-signal counterpart. A gate bias equal in polarity to the drain voltage impressed between gate and source will, once threshold had been passed, control the drain current.

When using a power DMOSFET, we need to be aware of its unipotential characteristic. A careful review of Figure 1.18 identifies a pn junction existing between drain and indirectly to the source by way of the body diffusion and the source-body bridge. Consequently an n-channel DMOSFET operates with only a positive drain potential and a p-channel DMOSFET with only a negative drain potential.

Because of velocity saturation, the gain of the device is high even with a gate-source voltage only slightly greater than the threshold voltage. Low-power DMOSFETs capable of offering drain currents of a few hundred milliamperes exhibit gain far in excess of their high-current JFET counterparts, and certainly higher than an equivalent-current, long-channel MOSFET—if one could be built in the first place.

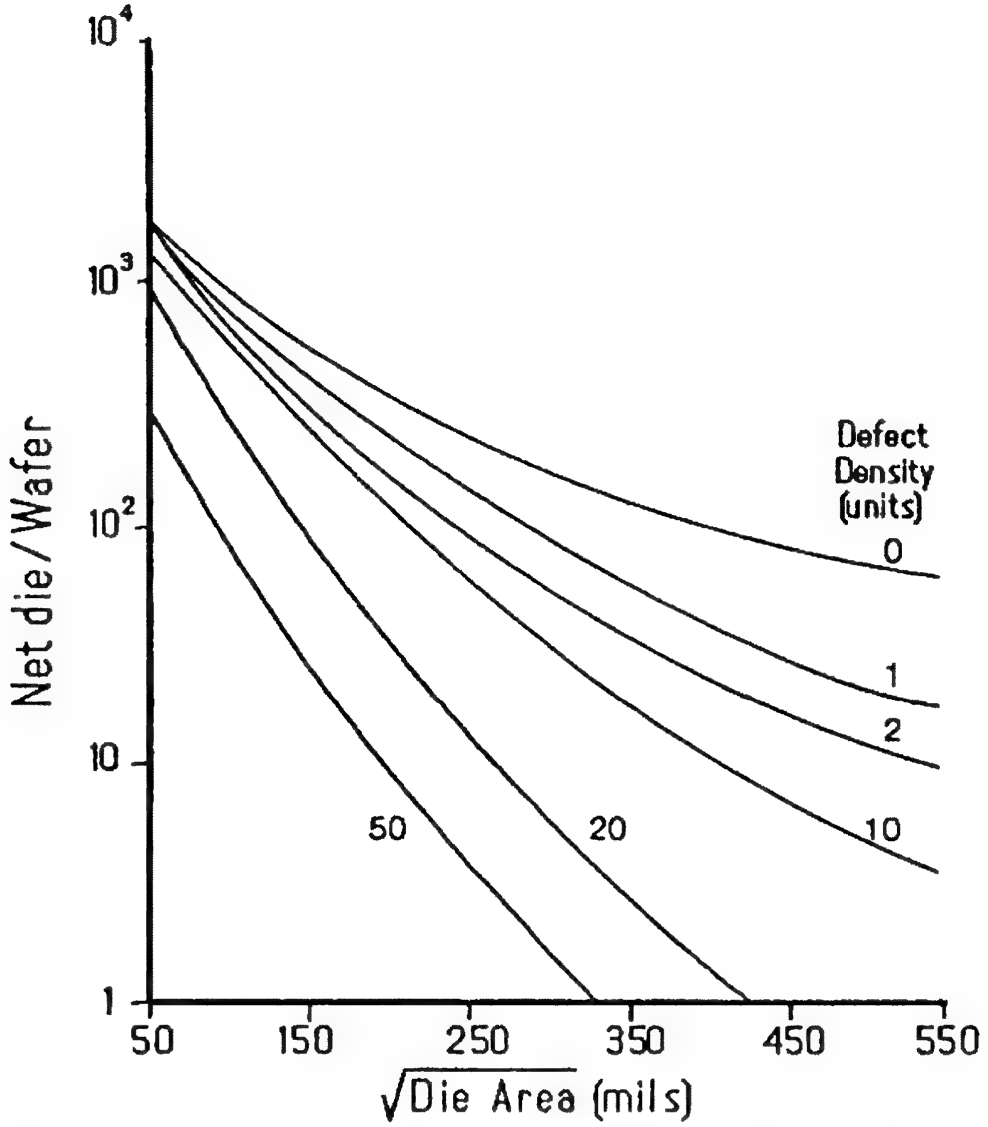

Figure 2.6 Net die yield per wafer is critically dependent on the absence of microscopic particulate matter. The effect becomes increasingly critical as die size enlarges. This effect is the fundamental limiting factor in the manufacture of large die semiconductors, which necessitates an ultraclean environment.

2.5 The Static-Induction Transistor

Although the static-induction transistor (SIT) might at first appear to be an outgrowth of the JFET; in performance it is not. Yet, it *is* a JFET—having a source, a drain, a diffused gate, and a short channel. As a result of this short channel, as with the DMOSFET, degeneration caused by excessive channel resistance is greatly reduced. What is immediately noticeable is that it, like the power DMOSFET, has a vertical current path. The SIT differs from the JFET in performance.

Current flow in the SIT between source and drain, rather than under the direct control of the depletion fields established by the gate-channel bias, is controlled by the height of an electrostatically induced potential barrier.

Unlike the conventional JFET, the majority carriers (electrons) travel at velocity saturation, which makes possible operation at very high frequencies. At the time of this writing, the SIT offers the potential of near-microwave performance with higher power and efficiency than currently are available using DMOSFETs.

However, like the JFET, the SIT, acting as we might expect of a depletion-mode device, requires an opposing gate-bias potential, thus necessitating two power supplies.

Quite unlike either the JFET or the DMOS, the static d-c characteristics of the SIT exhibit a triodelike characteristic, shown in Figure 2.7, rather than the more familiar pentode curve. Consequently, the SIT behaves much like the triode offering a more modest voltage amplification factor μ, as well as a considerably higher output admittance, g_{os} (quite obvious from Figure 2.7), than what we would expect of either a JFET or a DMOS.

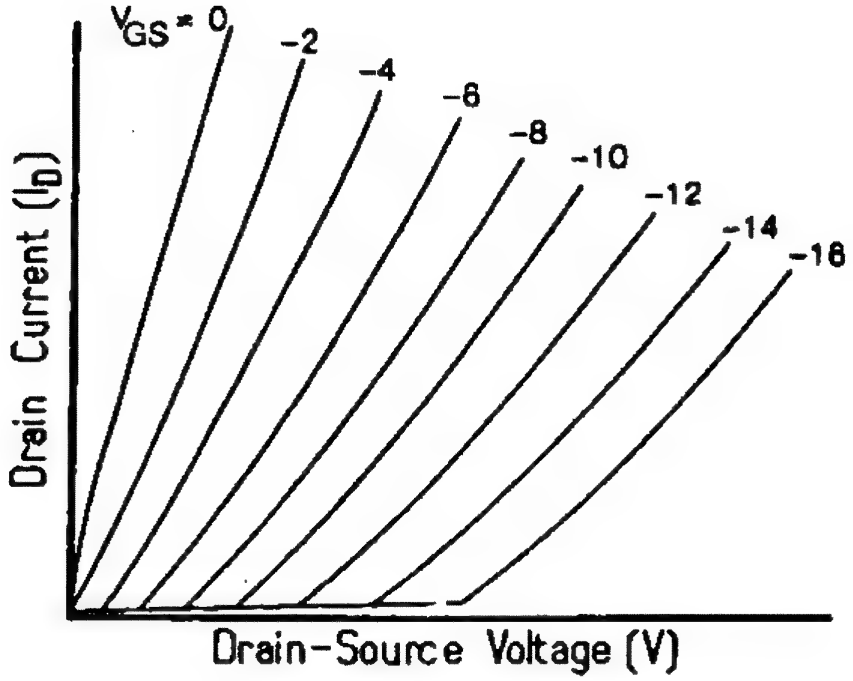

Figure 2.7 Output characteristics of the depletion-mode static-induction transistor.

2.6 The Insulated-Gate Bipolar Transistor

The popularity of the IGBT results from its high current density at high standoff voltages. Had the power DMOSFET not exhibited the deleterious r_{DS} versus $V_{(BR)DSS}$ phenomenon, as we saw in Eq. 2.3, the IGBT never would have materialized. Although it is certainly possible to manufacture a high-voltage, high-current power DMOSFET, to achieve the necessary low r_{DS} would require a proportionally larger chip. A large chip diminishes yields, escalating costs. That alone makes the high-voltage, high-power DMOSFET unsuitable for many applications. The IGBT offers high-voltage *and* high-current capabilities simultaneously, with a chip size considerably smaller than the equivalent power DMOSFET. A smaller semiconductor chip means higher yields and lower cost, and lower cost is a major attraction of the IGBT.

Operationally, the IGBT operates somewhat differently from the power DMOSFET. In review, the gate controls turn-ON, exactly as it does with the DMOSFET. It also allows control over turn-OFF, but, unlike the DMOSFET, where the control is both direct *and* near-instantaneous, turn-OFF for the IGBT exhibits the characteristic *storage time* of the power bipolar transistor! Also, unlike the power DMOSFET, the gate cannot be "crowbarred" to ground potential without possibly latching the IGBT.

A careful examination of Figure 1.20 should reveal why we have bipolarlike turn-OFF characteristics. The n-channel IGBT represented in this illustration has a p-doped substrate on which is grown an n-doped epitaxy, into which we build our conventional DMOSFET.

For the conventional power DMOSFET, this n-doped epitaxy, also called the *drain-drift region*, is what maintains the withholding (or breakdown) voltage. To increase the withholding voltage rating, we increase the resistivity of this epitaxy (hence the increase in r_{DS}).

However, with the n-channel IGBT we find this n-doped epitaxy has been grown on a p-doped substrate. If we carefully follow the current flow path, we discover that current is inhibited irrespective of direction by virtue of either the p-doped channel *or* the p-doped substrate. The former inhibits forward current; the latter inhibits reverse current flow. As a consequence, unlike the conventional power DMOSFET, we need not increase the resistivity of the n-doped epitaxy to achieve a higher withholding (breakdown) voltage.

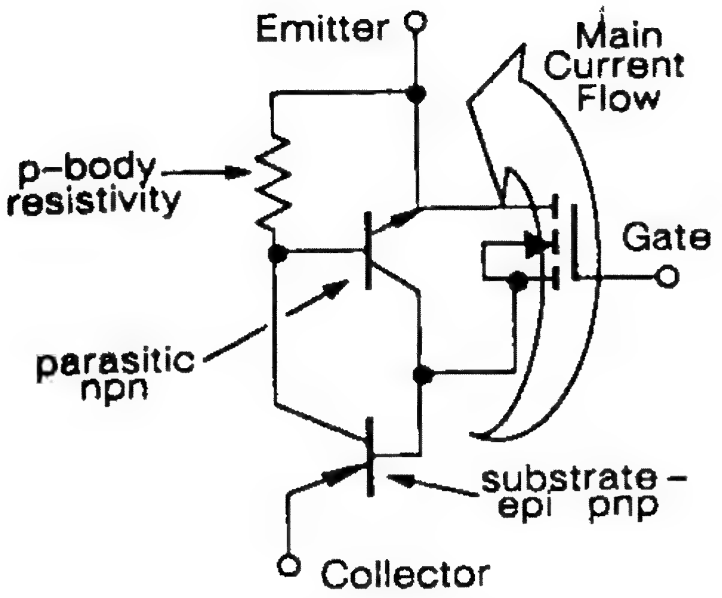

Figure 2.8 Equivalent circuit of the IGBT identifying the main current flow. The npn and pnp transistors may be identified in Figure 1.20.

Operation is best understood by examining the equivalent circuit shown in Figure 2.8. With a positive voltage on the collector (formerly the drain, when we considered DMOSFETs), when we bias the gate to induce carrier flow into this n-doped epitaxy region (see Figure 1.20) we flood (or *modulate*) the region with carriers (for an n-channel IGBT: electrons), forward biasing the p-n diode (p-substrate, n-epitaxial). Current flow is from the collector through the DMOSFET channel to the n^+ emitter.

Some confusion regarding the operation of the IGBT may be dispelled by careful study of Figure 2.8, where we discover that the *collector* is, in reality, the *emitter* of the substrate-epitaxy pnp bipolar transistor. The positive "collector" voltage *forward* biases the emitter-base junction, which results in the conductivity modulation. Conversely, a p-channel IGBT has an npn emitter acting as its collector.

Since we do not need to increase the resistivity of the n-doped epitaxy proportionally with increasing breakdown voltage (see Eq. 2.3), as would have been necessary with the more conventional DMOSFET, the current density is comparable to that of the p-n diode! Because of this, we have a MOS-gated structure both capable of high withholding voltages and able to handle large currents. In fact, if we allow a voltage drop of only a few volts—as we might also "allow" for a power DMOSFET—across "drain to source" (for the IGBT the bipolar nomenclature "collec-

tor to emitter" is used), the current density can easily exceed that of a power bipolar transistor 5 times and a power DMOSFET 20 times! Figure 1.21 compares an IGBT, a bipolar transistor, and a power DMOSFET.

Although this p-doped substrate with the n-doped epitaxy together inhibits reverse-current flow, it also inhibits the IGBT from competing with the conventional power DMOSFET at competitive breakdown voltages for reasons we have discussed in Chapter 1.

Although the IGBT offers high-power operation at reasonable cost, we must not lose sight of the storage time. Having flooded the n-epitaxy region with carriers, at turn-OFF we must allow a finite time for these carriers to either bleed off or recombine. Unlike the power DMOSFET, the IGBT is *not* a high-speed switch. For most applications, 20 kHz approaches the upper switching limit.

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3

Interpreting the Symbols

3.1 Introduction

In our quest to understand the specifications used to define the FET, one major stumbling block may be the interpretation of the symbology used to define electrical parameters. What exactly does a term such as I_{DSS} mean? Although we may not cover *every* symbol in this chapter, we will certainly blanket those we should expect to see when reading a FET data sheet.

This chapter is devoted in its entirety to the interpretation of the symbology that appears on every data sheet. Chapter 4 takes each symbol covered in Chapter 3 and defines how each parameter (for which the symbology is given) is achieved. Then Chapter 5 continues with a discussion of how these parameters affect performance and how the parameters interact with one another. As we proceed, we cannot avoid repeating some of what we have said previously.

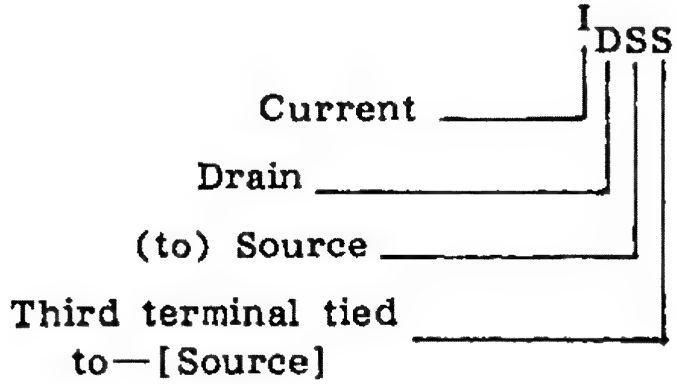
3.2 Interpreting the Symbols

Much time would be saved if there were simple rules to memorize. Unfortunately, such is not the case. Although there are some rules, contradictions abound, and there are a plethora of exceptions. One rule worthy of our study involves how to interpret subscripted letters, for example, in I_{DSS}.

The nonsubscripted capital letter, I, obviously stands for current. But what current? Our first subscripted letter, D, identifies that current as drain current. Our second subscripted letter, S, informs us that the drain current is flowing to the source. Therefore, I_{DS}, means drain-to-source current. However, we have a third subscripted letter.

The majority of transistors are three-terminal devices. Bipolar transistors have a collector, a base, and an emitter. FETs have a drain, a gate, and a source. Of course, some MOSFETs also have a body terminal as well; but that gets us into the exceptions sooner than we planned! For now, we need to know that the third subscripted letter identifies the location of attachment of the "unused" third terminal.

Thus if I_{DS} represents drain-source current, it is reasonable to say that two terminals out of three are in use: the drain and source terminals. That leaves the gate terminal, which, according to the third subscripted letter, S, is attached to the source. The term I_{DSS} simply means that with the gate tied to the source (zero gate bias, $V_{GS} = 0$), we have a measure of the zero-biased drain-source current.



Few symbols can have such diverse interpretations as does I_{DSS}. In *every* case, literally interpreted, we are specifying a zero-gate-biased, drain-source current. Yet, if we compare the specifications, which this symbol identifies, of a depletion-mode FET (whether JFET or MOSFET) and an enhancement-mode MOSFET, we discover that for the depletion-mode device we are measuring *maximum* current, but for the enhancement-mode FET the current is merely *leakage*!

Aside from the triple subscript symbol, as we have noted, other symbols offer a variety of information. Familiarity with these various and diverse symbols will help to qualify the reader's grasp of the transistor's capabilities.

3.3 A Glossary of Symbols

Many, if not all of these symbols were established by JEDEC, the Joint Electron Device Engineering Council (now called the Solid-State Products Engineering Council) of the Electronic Industries Association, in Washington, DC. The simplified definitions offered in this chapter, however, are those of this author. If the reader is surprised not to see some familiar symbols, such as V_{GS}, for "voltage, gate to source," it is only because the simple symbols really do not need interpretation.

3.3.1 Symbols for Voltage

$V_{(BR)DSS}$ Breakdown Voltage, Drain to Source, Gate Tied to Source

Also called avalanche breakdown. This symbol has, on many data sheets, replaced BV_{DSS}.

$V_{(BR)GSS}$ Breakdown Voltage, Gate to Source, Drain Tied to Source

Generally applied only to small-signal FETs. On many data sheets this symbol replaces BV_{GSS}.

$V_{DS(on)}$ Saturation Voltage, Drain to Source

The voltage drop across drain to source when the FET is in its full ON state. Also identified as $V_{DS(sat)}$, or V_{SAT}. This term is generally applicable to power transistors only.

$V_{GS(f)}$ Gate-Source Forward Voltage

Applicable to JFETs only. A measure of the voltage drop across the gate junction when forward gate (diode) current I_G, usually a few milliamperes) is forced.

$V_{GS(off)}$ Gate Cutoff Voltage

The gate-to-source voltage of a depletion-mode FET (or MOSFET) as the channel conductance approaches cutoff. This voltage is

measured at an arbitrary, but convenient level of cut-OFF current (but greater than the leakage current). The polarity of the voltage is always opposite that of the drain voltage.

$V_{(GS)th}$ *Threshold Voltage, Gate to Source*

Also may be shown as V_T, V_{TH}, and $V_{(th)}$. The gate-to-source voltage of an enhancement-mode MOSFET that is required to achieve channel conduction. This voltage is measured at an arbitrary, if not convenient value of turn-ON drain current. The polarity of the voltage matches that of the drain potential.

V_p *Pinch-OFF Voltage*

Refer to the discussion leading to Eq. 2.1 in Chapter 2.

3.3.2 Symbols for Current

$I_{A(R)}$ *Avalanche Current*

Associated with unclamped inductive testing of power DMOSFETs, $I_{A(R)}$ identifies the maximum avalanche current during switch-OFF. The (R) stands for "repeated measurement." The magnitude is generally equal to the I_D rating of the power DMOSFET.

I_D *Continuous Drain Current*

Although widely accepted as the maximum root-mean-square operating drain current for a power DMOSFET, the value is generally calculated as follows:

$$I_D = \left(\frac{P_D \text{ @ } T_A}{r_{DS(on)} \text{ @ } T_J} \right)^{1/2} \tag{3.1}$$

To measure I_D at the normal operating drain voltage would necessitate a pulsed test to avoid exceeding the dissipation of the transistor.

$I_{D(on)}$ *ON-State Drain Current*

Although equivalent to I_D, it is measured at considerably lower voltages (and often under pulse conditions) to ensure that the transistor's power rating is not exceeded.

It is this symbol we use to identify the minimum drain-source current of an enhancement-mode MOSFET, rather than the symbol I_{DSS}, which is used for depletion-mode FETs.

$I_{D(off)}$ *Drain Cutoff Current*

Identifies the OFF current through a JFET when biased beyond cutoff. The term denotes the leakage current through the JFET.

I_{DM} *Pulsed Drain Current*

The maximum drain current that is feasible for the FET when the gate is biased to full ON. The current must be pulsed to guard against exceeding both the dissipation and the safe operating area.

I_{DSS} *Zero-biased Drain Current*

For a depletion-mode FET, this term identifies the saturated drain current. For an enhancement-mode MOSFET, the term identifies the leakage current.

I_G *Operating Gate Current (of a JFET)*

Not to be confused with I_{GSS} (see next definition), where the JFET is *not* operational. This parameter depends on V_{DG} (*not* V_{DS}) and I_D, as well as, of course, the polarity of the gate voltage V_{GS}. The input (gate) resistance of a JFET (with the polarity of V_{GS} in the reverse-biased condition, vis., for an n-channel JFET, negative) may be approximated using the equation:

$$R_G = \frac{V_{DG}}{I_G} \qquad (3.2)$$

I_{GSS} Gate-to-Source Current, Drain Tied to Source

This parameter always represents a *leakage* current, consequently the impressed voltage across gate to source is reverse biased. For a JFET (or SIT) where the gate channel is a pn junction, the positive potential appears at the n-doped region.

For MOSFETs, the polarity is of lesser importance.

Note that the FET is *inoperable* because the drain is electrically tied to the source.

I_S Continuous Source Current

A term used in the characterization of the body-drain diode of a power DMOSFET.

3.3.3 Symbols for Resistance

$R_{DS(on)}$ Static Drain-Source ON-State Resistance (also shown as $r_{DS(on)}$)

With the gate held at a specified voltage to ensure that whatever change we have in drain-source voltage, V_{DS}, will correspond to a proportional change in drain current, I_D, (Ohm's law). This mandates that the FET be in its linear (triode) region of operation, where V_{DS} is less than V_p, and also less than $V_{GS} - V_{GS(off)}$.

$r_{ds(on)}$ Dynamic Drain-Source ON-State Resistance

In essence, this is identical to the static form, but conducted as an ac measurement.

R_{thJC} Thermal Resistance, Junction to Case (also identified as $R_{\theta JC}$)

By the amount of thermal resistance that exists between the semiconductor chip and its header (package), we see a corresponding rise in temperature per unit power dissipation with respect to the temperature of an external reference.

R_{thCS} Thermal Resistance, Case to Sink (also identified as $R_{\theta CS}$)

By the amount of thermal resistance existing between the semiconductor's package (case) and the heatsink to which it has been firmly attached, we see a corresponding rise in temperature per unit power dissipation with respect to the temperature of an external reference.

R_{thJA} Thermal Resistance, Junction to Ambient (also identified as $R_{\theta JA}$)

The summation of R_{thJC}, R_{thCS}, and the thermal resistance existing between the heatsink and free air (R_{thSA}) at whatever temperature this free air (ambient) is.

Taken together, we can provide an electrical analog circuit of the thermal resistance, shown in Figure 3.1.

3.3.4 Symbols for the Dynamic Characteristics

g_{fs} Forward Transconductance

Also identified as g_m. This symbol indirectly identifies the gain of the FET.

With power FETs, this dimension is given in Siemens (formerly mhos).

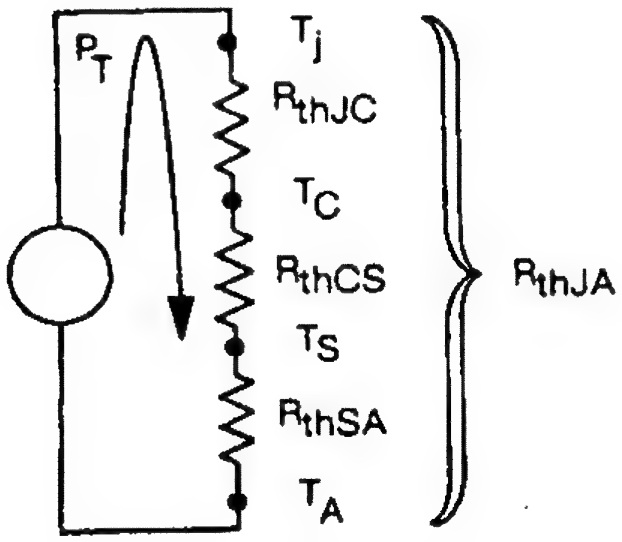


Figure 3.1 Electrical analog of thermal resistance for a typical semiconductor, where P_T represents the total power dissipated by the FET.

g_{os} Output Conductance

The rate of change of drain current to drain voltage, expressed by the equation:

$$g_{os} = \frac{dI_D}{dV_{DS}} \tag{3.3}$$

Although this term is generally applied to small-signal FETs, it does identify the *slope* of the output characteristic curves in the saturated region of any FET.

C_{iss} Input Capacitance, Input (Gate) to Source

The third subscript indicates that the drain should be tied to the source. Because the drain is tied to the source, the actual value of input capacitance includes C_{gs} plus C_{gd}!

$$C_{iss} = C_{gs} + C_{gd} \tag{3.4}$$

C_{oss} Output Capacitance, Output (Drain) to Source

The third subscript indicates that the gate should be tied to the source, resulting in a total output capacitance of the parallel combination of C_{ds} and C_{gd}:

$$C_{oss} = \frac{C_{ds} \cdot C_{gd}}{C_{ds} + C_{gd}} \tag{3.5}$$

C_{rss} Reverse Transfer Capacitance, Common Source

Identical to C_{gd}. This symbol is one of many exceptions to our rule, since neither the second nor the third subscript means what we previously learned.

$$C_{rss} = C_{gd} \tag{3.6}$$

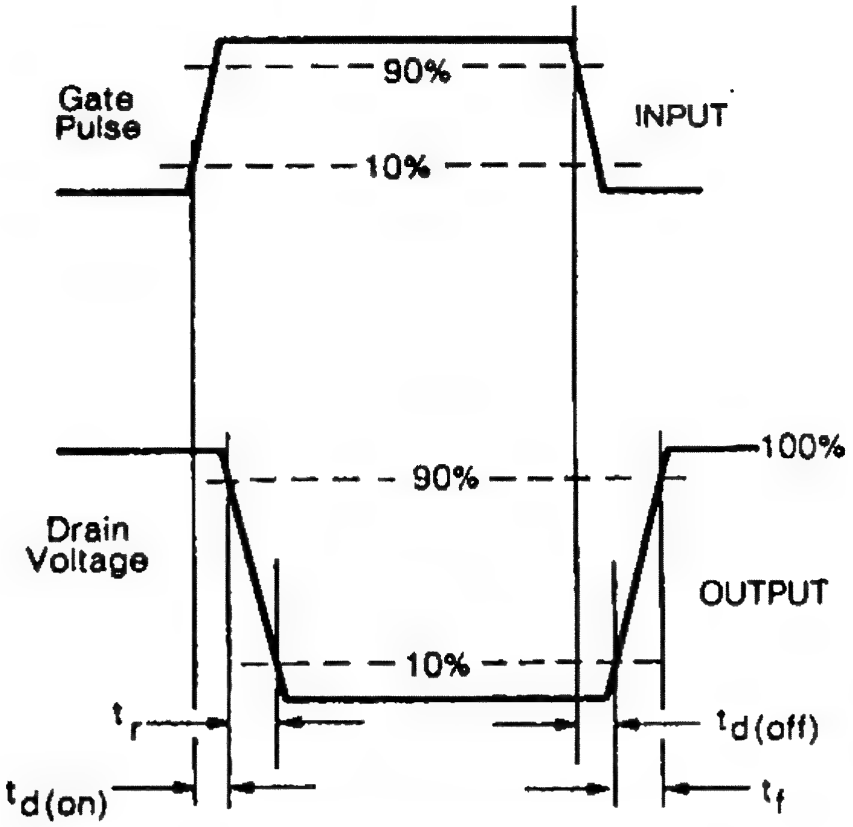


Figure 3.2 Switching waveforms.

$t_{d(on)}$ *Turn-ON Delay Time*

Interval of time beginning at the 10% rise time of the gate pulse to the moment when the drain voltage has dropped to 90% of its nonconducting state. See Figure 3.2.

t_r *Rise Time*

The interval of time during which the drain voltage has dropped *from* 90% to 10% of its nonconducting state. See Figure 3.2.

$t_{d(off)}$ *Turn-OFF Delay Time*

The interval of time beginning when the gating pulse falls to 90% of its peak value and ending at the moment of drain voltage rises to 10% of its OFF-state amplitude. See Figure 3.2.

t_f *Fall Time*

The interval of time during which the drain voltage has risen from 10% to 90% of its nonconducting state. See Figure 3.2.

t_{rr} *Reverse Recovery Time*

If the body-drain diode of a power DMOSFET has reason to enter into forward conduction, when the diode switches OFF, the current through the diode reverses momentarily. The time for this current to fall once again to 25% of its peak value is called the reverse recovery time. See Figure 3.3.

Q Charge (Figure 3.4)

Current is the rate of flow of charge, thus,

$$i = \frac{Q}{dt} \tag{3.7}$$

Furthermore, we know that

$$Q = C\ dV \tag{3.8}$$

so, combining Eq. 3.7 and Eq. 3.8, we have:

$$i = \frac{C\ dV}{dt} \tag{3.9}$$

Consequently, we place a charge on the FET gate to induce current flow, namely, a continuous "flow of charge" I_D. In the early days of power DMOSFETs it was customary to adjust the gate current by changing either the voltage or impedance of the gate drive. Because of the difficulty of specifying capacitance, however, achieving a foreknown switching speed was all but impossible.

$Q_{g(th)}$ *Gate Threshold Charge*

Identifies the minimum gate charge required *before* we reach the minimum threshold voltage. We are also able to identify the OFF-state value of C_{gs}. This symbol is used principally on power DMOSFET data sheets.

$Q_{g(on)}$ *ON-State Gate Charge*

Identifies the minimum gate charge necessary to ensure the correct measurement of $r_{DS(on)}$.

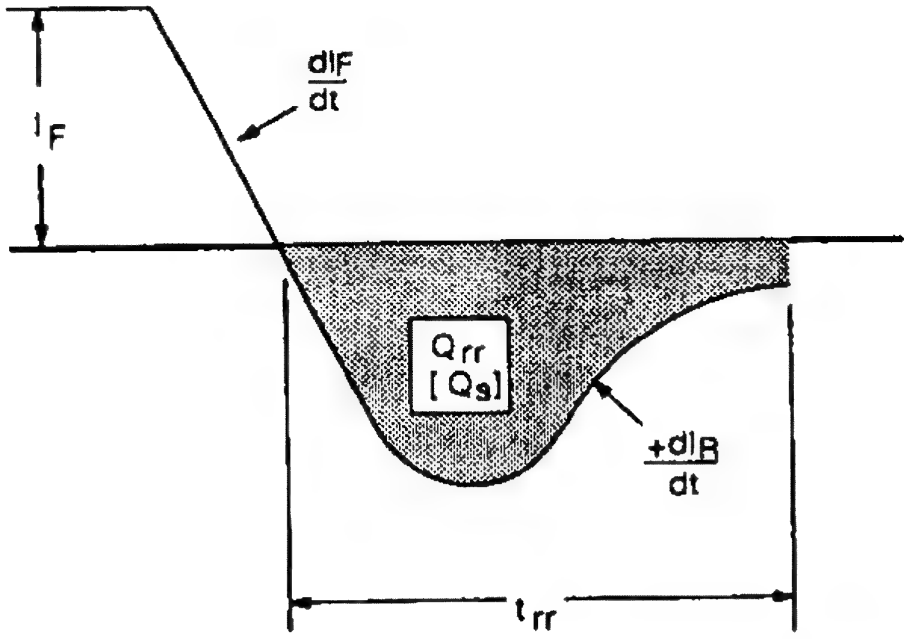


Figure 3.3 Reverse recovery time of the parasitic body-drain (DMOSFET) diode. Note that Q_{rr} is also called Q_s.

This symbol is generally found on power DMOSFET data sheets.

$Q_{gm(on)}$ *Peak ON-State Gate Charge*

Identifies the minimum gate charge required to reach the maximum gate-source voltage.

3.3.5 Miscellaneous Symbols

There are many symbols to identify specific applications. For example, we have FETs characterized for both low- and high-frequency amplifier service, dual JFETs for use as input buffers for operational and differential amplifiers, smoke detectors . . . the list is endless.

The few symbols offered here are frequently seen on data sheets.

e_n *Short-Circuit Equivalent Input Noise Voltage*

Closely approximates the equivalent thermal noise voltage of the channel resistance (with the exception of so-called low flicker

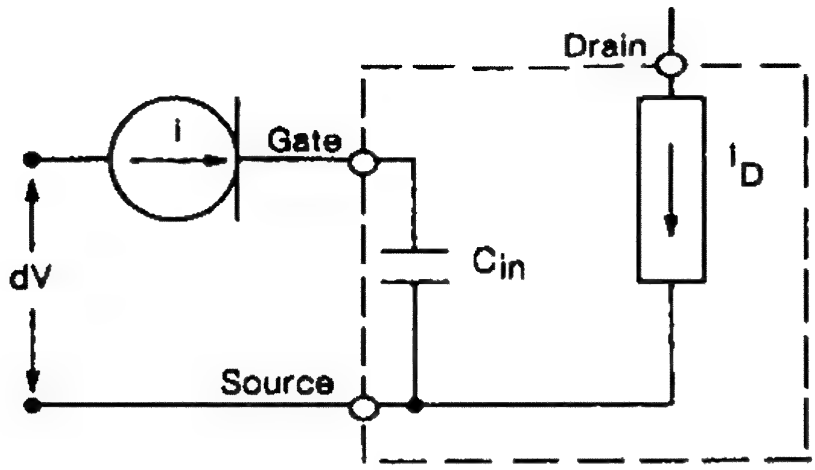


Figure 3.4 Basic equivalent circuit of a charge-controlled FET.

noise $1/f^n$). This symbol is generally found on data sheets of small-signal JFETs designed especially for amplifier service.

We may define this noise voltage as follows:

$$\bar{e}_n = (4kTR_NB)^{1/2} \tag{3.10}$$

where

k = Boltzmann's constant
T = temperature in degrees Kelvin
B = bandwidth in Hertz
R_N = equivalent input noise resistance; for an n-channel JFET, the value approaches:

$$R_N = \frac{0.67}{g_{fs}} \tag{3.11}$$

In what is called the $1/f^n$ region, the noise voltage is expressed as follows:

$$\bar{e}_n = \left[4KR_NB\left(1 + \frac{f_1}{f^n}\right)\right]^{1/2} \tag{3.12}$$

where n (in f^n) varies between 1 and 2.

Figure 3.5 identifies the equivalent noise circuit of an idealized JFET.

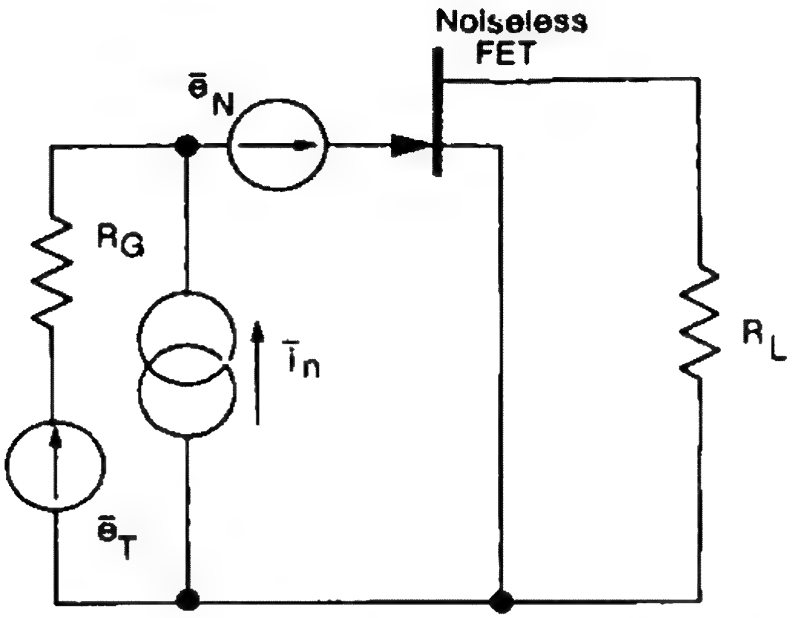


Figure 3.5 Basic equivalent circuit representing noise in an ideal JFET.

The noise characteristics of a JFET are frequency dependent and take the form shown in Figure 3.6.

NF Noise Figure

Expressed in decibels (dB). Careful inspection of Figure 3.5 shows an additional source of noise, identified as $\bar{i}_n$, that is in shunt with the input. Together with $\bar{e}_n$, we can define the noise *power* of the JFET as follows:

$$N_p = \frac{\bar{e}_n^{\,2}}{R_G} + \bar{i}_n^{\,2} \cdot R_G \qquad (3.13)$$

Defining the low-frequency noise figure of a JFET is somewhat awkward because it must *always* be given with reference to some standard, which, as we have seen from Eq. 3.13, the generator resistance R_G:

$$NF = 10 \log \left(1 + \frac{\bar{e}_n^{\,2} + \bar{i}_n^{\,2} R_G^{\,2}}{4kTR_GB} \right) \qquad (3.14)$$

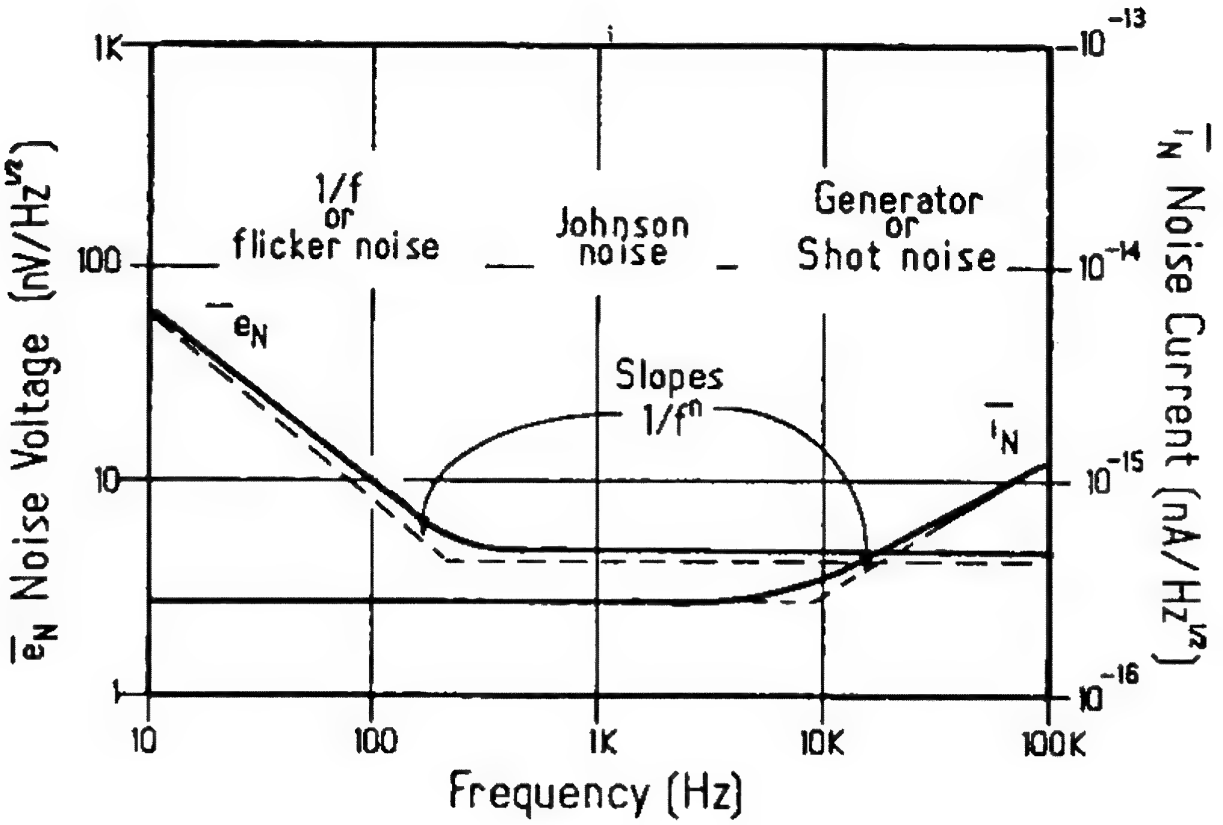


Figure 3.6 Characteristics of JFET noise.

For this reason, $\bar{e}_n$ is the more popular expression for defining the noise of a JFET.

Figure 3.7 offers a simple conversion between noise figure and noise voltage, e_n, if the source (or generator R_G) resistance is known. Since this conversion omits the term $\bar{i}_n$, of Eq. 3.14, it is valid only when the operating gate current I_G, is very low (generally always the case at audio frequencies).

Noise figure may also identify the high-frequency performance of a FET. Quite often we find no reference to R_G on the data sheet, although, in general, 50 Ω is assumed.

Yet, we must be aware that the assumption of 50 Ω does *not* mean that the FET in question performs with an R_G of 50 Ω. It means only that the FET has been impedance-matched to 50 Ω. Its true source resistance to achieve the specified noise figure is seldom offered.

dV/dt

Generally identified by symbol. It represents the slew rate of drain voltage possible before a latch-up condition occurs. This latch-up may result in destruction of the DMOSFET.

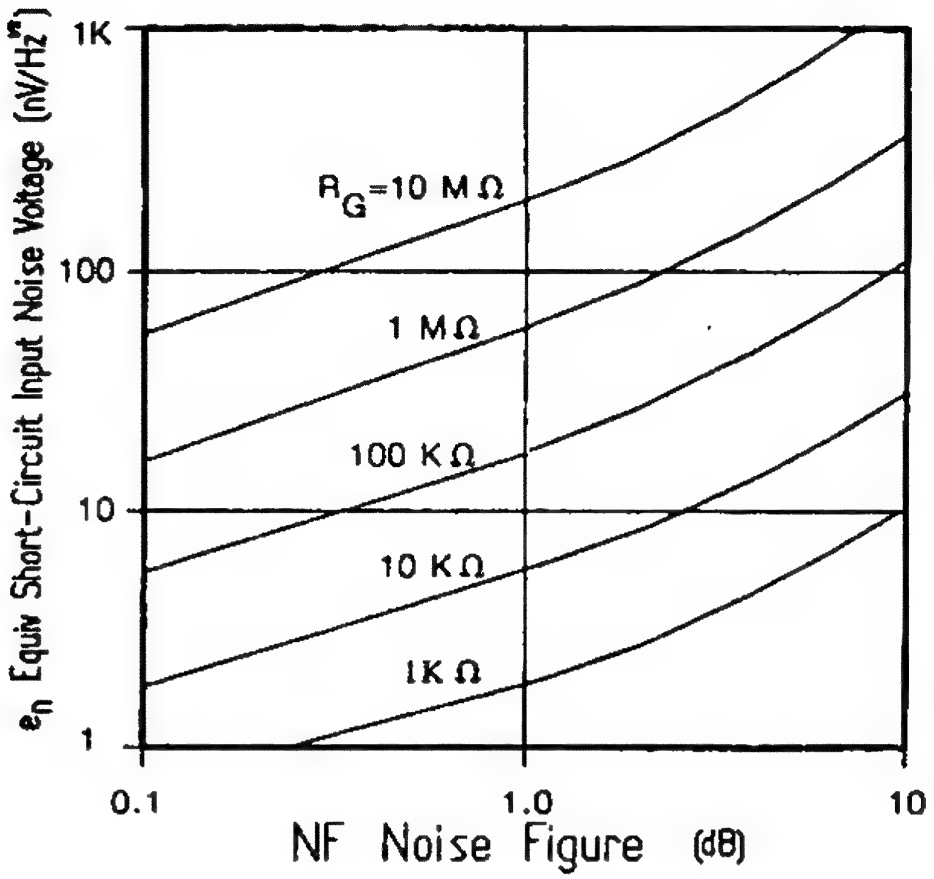


Figure 3.7 Chart for converting noise voltage to noise figure. Useful for JFETs, where we may assume zero noise contribution from generator recombination (or shot) noise (i_n = 0 in Eq. 3.14).

Symbols for Degree of Electrical Match

Additionally, we find symbols used to identify the matching parameters of dual-packaged JFETs (and some small-signal MOSFETs). These symbols, consisting, for the most part, of symbols we have just defined, identify the degree of electrical match. Rather than repeat our definitions, the following is self-explantory.

$|V_{GS1} - V_{GS2}|$ *Differential Gate-Source Voltage*
Expressed in millivolts for a common drain current.

$\Delta|V_{GS1} - V_{GS2}|/\Delta T$ *Gate-Source Voltage Differential Drift*
Expressed in microvolts per degree Celsius where ΔT is generally offered between −55°C to 25°C and 25°C to 125°C.

g_{fs1}/g_{fs2} *Transconductance Ratio*

We are likely to find other combinations of symbols which, hopefully, will be self-explanatory.

Appendix A

JEDEC Standard No. 24 defines the terms, definitions, and letter symbols for power MOSFETs.

Appendix B

Military Standard MIL-STD-750C provides detailed testing procedures for all discrete semiconductors. The methods specifically pertaining to power MOSFETs include the following.

Environmental tests (1000 series)
Mechanical characteristics tests (2000 series)
Circuit performance and thermal resistance measurements (3100 series)
- 3141 Thermal response time
- 3161 Thermal impedance measurements for vertical power MOSFETs (delta source-drain voltage method)

Electrical characteristics tests for field-effect transistors (3400 series)
- 3401 Breakdown voltage, gate to source
- 3403 Gate-to-source voltage or current
- 3404 MOSFET threshold voltage
- 3405 Drain-to-source ON-state voltage
- 3407 Breakdown voltage, drain to source
- 3411 Gate current
- 3413 Drain current
- 3415 Drain reverse-current
- 3421 Static drain-to-source ON-state resistance
- 3459 Pulse response
- 3470 Unclamped inductive switching
- 3471 Gate charge
- 3472 Switching time test
- 3473 Reverse recovery time
- 3474 Safe operating area
- 3475 Forward transconductance, pulsed d-c method
- 3476 Diode recovery dv/dt

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4

Characterization, Part I

How Parameters Are Achieved

4.1 Introduction

Chapter 3 identified most if not all of the important symbols we should expect to find as we review any FET data sheet. Every symbol represents a measurable parameter. This chapter focuses on how each parameter is achieved.

Like the earlier chapters, Chapter 4 offers phenomenological explanations without recourse to mathematics that might overcome the reader. Again, should the inquisitive reader wish to dig deeper, the references at the end of the chapter may be consulted.

4.2 How Each Parameter Is Achieved

We begin as we did in the preceding chapter, but rather than expanding on the interpretation of every symbol, we uncover the significance of each parameter that a symbol represents. In other words, we try to develop a better understanding of each parameter.

Those familiar with the design and manufacture of FETs recognize that what follows is far from a rigorous exercise. Likewise, it is understood that these parameters are interwoven; that is, few stand alone without compromising other parameters. But how they compromise each other is left for Chapter 5.

4.2.1 $V_{(BR)DSS}$ *Avalanche Breakdown*

This symbol is replacing BV_{DSS} on many data sheets.

JFET

Because of the symmetrical nature of most small-signal JFETs, $V_{(BR)DSS}$ (formerly BV_{DSS}) is seldom used to define breakdown since, by definition (see Section 3.3.1) the gate is electrically tied to the source. As a consequence, such a test would provide breakdown data between the drain and gate only.

DMOSFET

A careful review of the cross-section of an enhancement-mode power DMOSFET reveals two possibly unexpected facts. First, the channel itself does not directly contribute to the breakdown voltage; and, second, breakdown appears to be not so much a MOSFET parameter but a *diode* parameter! This becomes clear if we study Figure 4.1, where we discover that the drain-source breakdown phenomenon impinges principally on the pn region and the associated resistivities that together make up the DMOSFET.

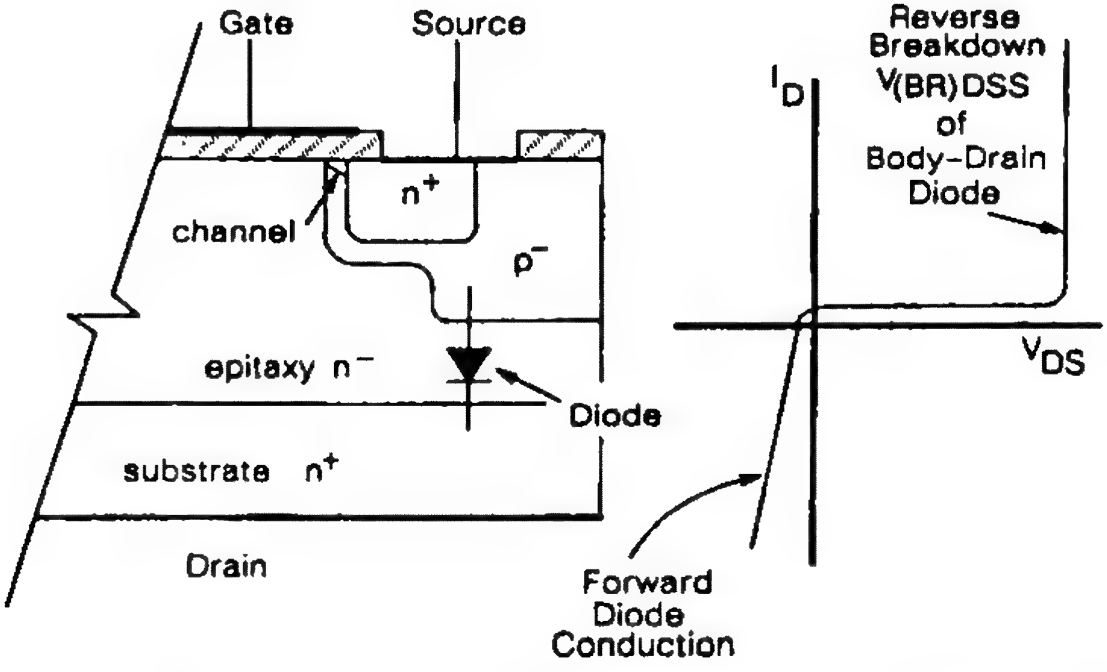


Figure 4.1 Breakdown in a vertical power DMOSFET occurs across the pn junction between the p^- diffusion and the n^- epitaxy.

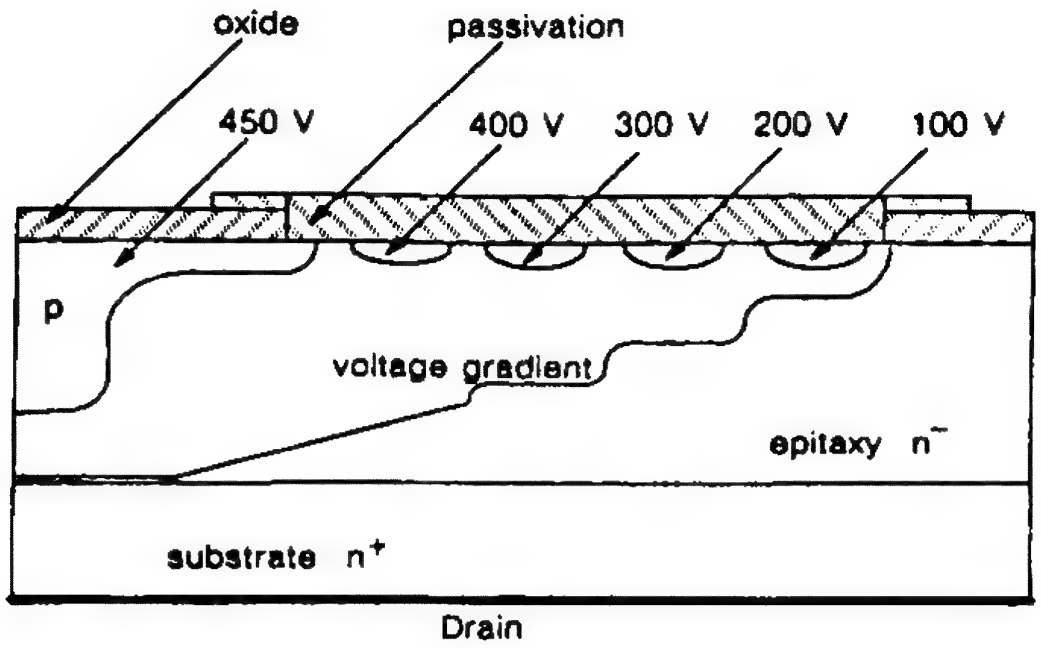


Figure 4.2 The idealized guard ring design.

Compensation for depletion-layer curvature is common for all power transistors, and the power DMOSFET is not an exception. Diffused guard rings, diffused field-limiting rings, and field plate structures find wide appeal in designing high-voltage structures. Figure 4.2 presents a hypothetical cross-sectional view of a transistor compensated for depletion-layer curvature.

SIT (Static-Induction Transistor)

This high-voltage JFET equivalent exhibits its extraordinary breakdown characteristics because of its thick epitaxial layer between gate and drain.

Despite the high-power nature of the SIT, the breakdown characteristics of this device more probably resemble those of the JFET than those of the power DMOSFET.

Yet, like all power transistors, it suffers from depletion-layer curvature, requiring compensation not unlike that used for any high-voltage, high-power transistor. Of the three possible cures, the field plate appears more widely used.

IGBT (Insulated-Gate Bipolar Transistor)

Even though the IGBT has what amounts to an n-p-n-p diffusion, to maintain high breakdown characteristics, we must follow the rules of the power DMOSFET.

To achieve a high breakdown potential between collector (drain) to gate, various junction-curvature schemes must be used.

However, quite unlike the power DMOSFET, if we wish to achieve a high *reverse* breakdown characteristic (vis., placing a reverse-polarity charge on the collector/drain), special care must be taken in fabrication to ensure a defect-free edge between substrate and epitaxy. The sawn edge of Figure 1.20 guarantees little if any reverse-polarity capability. One possible solution might be to surround the vertical p-n-p-n structure in a dielectric medium of intrinsic silicon.

4.2.2 $V_{(BR)GSS}$ *Avalanche Breakdown, Gate to Source*

This symbol is replacing BV_{GSS} on many data sheets.

JFET (only)

With drain tied to source, $V_{(BR)GSS}$ (formerly BV_{GSS}) clearly identifies the avalanche breakdown characteristics of a symmetrically diffused JFET. Breakdown occurs in the gate-drain/source depletion regions. As a consequence, we see a definite relationship between the breakdown voltage and the gate-source voltage V_{GS}, as shown in Figure 4.3.

Additionally—and this is generally universal among semiconductors—the effects of junction (depletion-layer) curvature play a major role in the breakdown voltage. The shallower the diffusion, the greater the curvature and the lower the breakdown voltage.

Small-signal JFETs and MOSFETs not only are physically quite small but seldom are compensated for the ravages of this effect. As a consequence, most small-signal FETs have low breakdown voltage ratings, generally under 60 V.

There is, however, a class of JFET purposely designed with an off-center gate diffusion offering extremely low degeneration (the 2SK19 and the 2SK152, among others); for this case, $V_{(BR)GSS}$ may be considerably less than $V_{(BR)DSS}$. For this special class, $V_{(BR)DSS}$ might be a more suitable measure of performance.

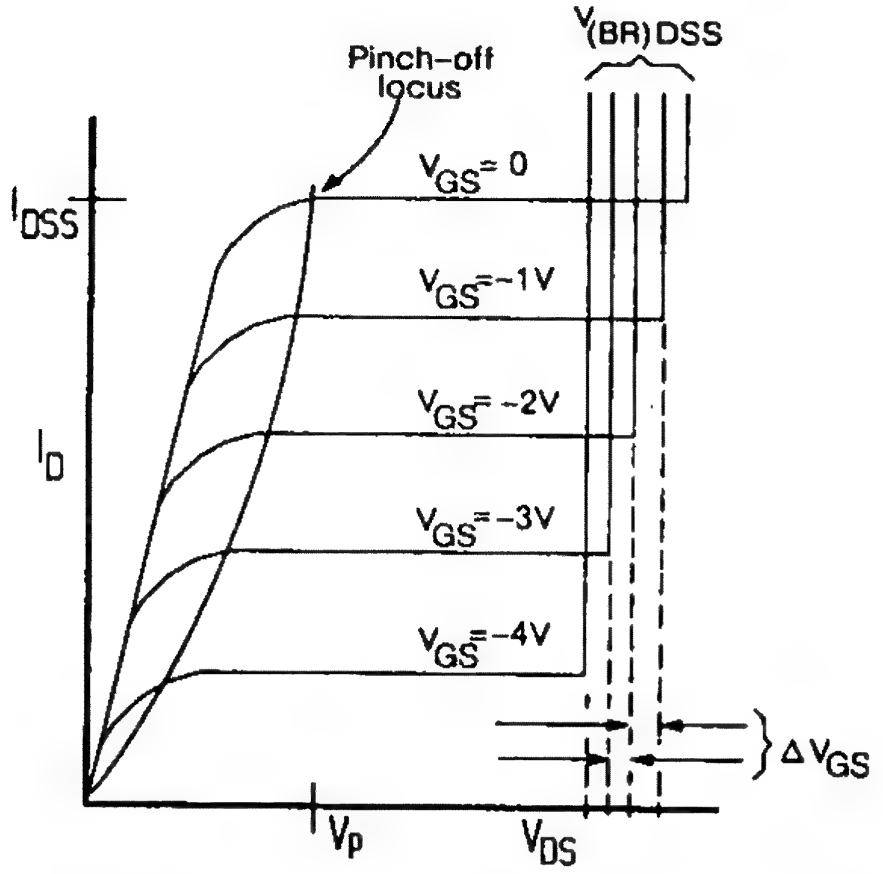


Figure 4.3 Since JFET breakdown occurs between drain and gate, a direct dependency exists between V_{GS} and V_{DS} where breakdown directly follows the change in gate bias.

4.2.3 $V_{DS(on)}$ *ON-State Drain-Source Voltage*

Until early in 1985 this specification had been a sensitive issue, with power MOSFET vendors trying to compete with power bipolar transistors. Since this specification reflects nothing more than the product of drain current I_D and ON-resistance $r_{DS(on)}$, our only control to lower $V_{DS(on)}$ is to design a low-ON-resistance DMOSFET.

This parameter is, in effect, a measure of the power transistor's efficiency, hence the former sensitivity among competing vendors. The product of voltage $V_{DS(on)}$ and current I_D gives the heat loss within the device, and, indirectly, becomes a measure of efficiency.

4.2.4 $V_{GS(f)}$ *Gate-Source Forward Voltage*

During assembly of the JFET die into the package (header), when no top gate bond is used, a satisfactory result of this test

ensures that the gold eutectic die attach has not cause a Schottky (Au-Si) diode barrier, which would result in an unacceptably high series gate resistance.

Testing for this parameter, we would expect to find one diode drop for a reasonable forward gate current. Generally anything exceeding 1 volt at a few milliamperes of forward gate current is cause for rejection.

4.2.5 $V_{GS(off)}$ *Gate-Source Cutoff Voltage*

JFET

In the fabrication process we have considerable lattitude in establishing the gate-source cutoff voltage by the seemingly simple process of controlling the depth of the gate diffusion. A shallow diffusion means a higher cutoff voltage, whereas a deep diffusion lowers the cutoff voltage.

The deeper we diffuse the gate, the more narrow becomes the active channel height and the smaller the depletion area that is required to effect cutoff. Consequently, for a deep diffusion we require less gate voltage to achieve cutoff, as we see in Figure 4.4.

MOSFET (Depletion-Mode)

Controlling the cutoff voltage is a multifaceted task involving several potential variables: the composition of the gate itself (metal or polysilicon or a combination), the composition and thickness of the gate oxide, and the channel doping density and thickness. An additional variable may be the substrate, which, when biased, may act in some ways as a parasitic gate.

A more serious consequence arising from the composition of both the gate and the oxide is its effect on developing electrostatic charges. These charges, often resident within the oxide, materially affect the gate cutoff voltage.

The specification for gate cutoff voltage applies only to depletion-mode FETs for obvious reasons. As the name suggests and from what we read in Chapter 2, by the application of a gate voltage we are depleting the channel. This can be accomplished only by reverse-biasing the gate (with respect to the polarity of the drain), whether the gate be diffused (a JFET) or oxide-insulated (a MOSFET).

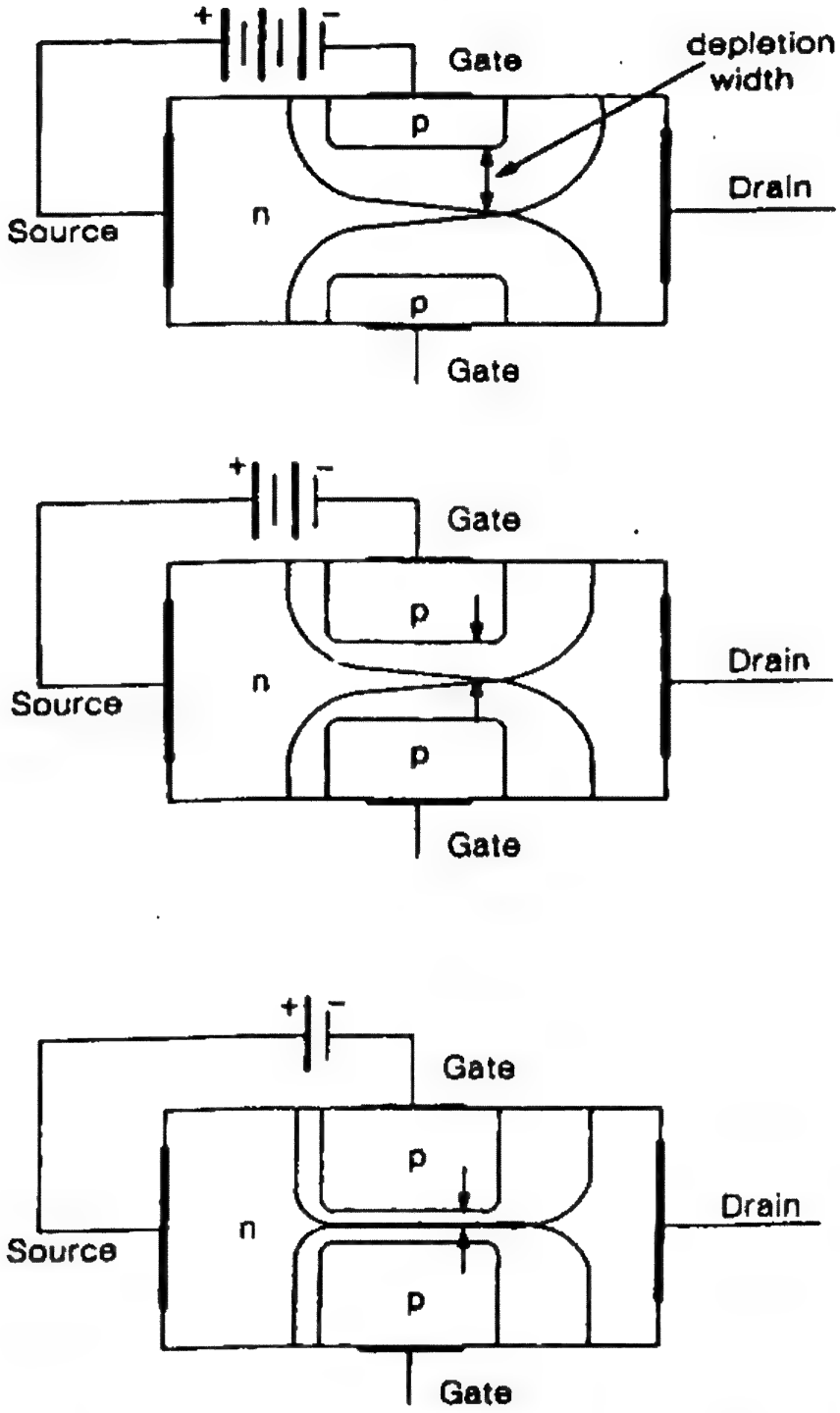


Figure 4.4 The more deeply the gate is diffused, the less gate voltage is needed to achieve cutoff.

4.2.6 $V_{GS(th)}$ *Threshold Voltage* [also identified by V_{th} and V_T]

Applicable only to enhancement-mode MOSFETs. To a great extent the pinch-off problems associated with the depletion-mode MOSFET may be shared with the enhancement-mode MOSFET.

However, we recognize that the enhancement-mode MOSFET really does not have an active channel until one is created by the application of the correct gate bias polarity. This we learned in Chapter 2.

Consequently, an additional restraint on this parameter focuses on the creation of the current conduction channel. Again, as with the depletion-mode MOSFET, charges resident within the gate oxide play a crucial role in the establishment of the threshold voltage. If, for example, we consider an n-channel MOSFET, these resident charges are electrons; then their inhibiting effect on the creation of a channel must be overcome by the applied (positive) gate bias. A major problem in manufacture is contamination, the most common source being positive sodium ions, which lower the threshold voltage. Additionally, a variety of "fixed" (usually positive) charges may contaminate the gate oxide, also contributing to the lowering of the threshold voltage of n-channel MOSFETs. Consequently, these, along with myriad other problems, lead to the creation of what the manufacturer identifies as the threshold voltage.

The threshold voltage found on a data sheet is merely a gate-source voltage required to produce a small drain current. The published value is *not* the true threshold one might need in modeling.

4.2.7 V_p *Pinch-off Voltage*

JFET

In Chapter 2 we examined in some detail how the pinch-off voltage is derived. Instead of repeating this material here, we offer a phenomenological derivation that should support our previous statements.

In Figure 2.1 we saw that the depletion region blooms to effect a pinched-off condition when the drain-source voltage rises to some predetermined level, which we now know, from Chapter 2, to be equal in magnitude to $V_{GS(off)}$ (see Eq. 2.1).

If we presume our JFET to be built to be physically symmetrical, having the gate-source region equal to the gate-drain region, then we may presume, phenomenologically, that the drain-source voltage (with gate tied to source, thereby making $V_{DS} = V_{DG}$) should offer the same depletion-field effect as does the gate-source voltage V_{GS}.

Compare a positive drain voltage and negative gate/source (gate tied to source) to a negative gate voltage and positive

source. We have, in effect, equal magnitudes of bias but opposite polarity. Consequently, we agree that Eq. 2.1, repeated below, is correct!

$$|V_{GS(off)}| = |V_p| \tag{4.1}$$

Again, repeating from Chapter 2, if our JFET channel is extremely short, the drain voltage necessary to achieve pinch-off may exceed the gate-source voltage $V_{GS(off)}$. This results from an interesting phenomenon: the electrons "drifting" in the channel are accelerated by the influence of a strong positive electric field (drain). This, of course, is expected, but the short channel magnifies the effect, causing the carriers (electrons) to reach their critical (limiting) velocity. At this point, a stronger drain field has no further effect and carrier (current) saturation occurs. The effect is shown in Figure 4.5.

4.2.8 $I_{AI(R)}$ *Avalanche Current (Repetitive)*

This new parameter is a measure of the ruggedness of the power DMOSFET. With a specified load inductance (unclamped), the DMOSFET is switched OFF, allowing the drain voltage to surge

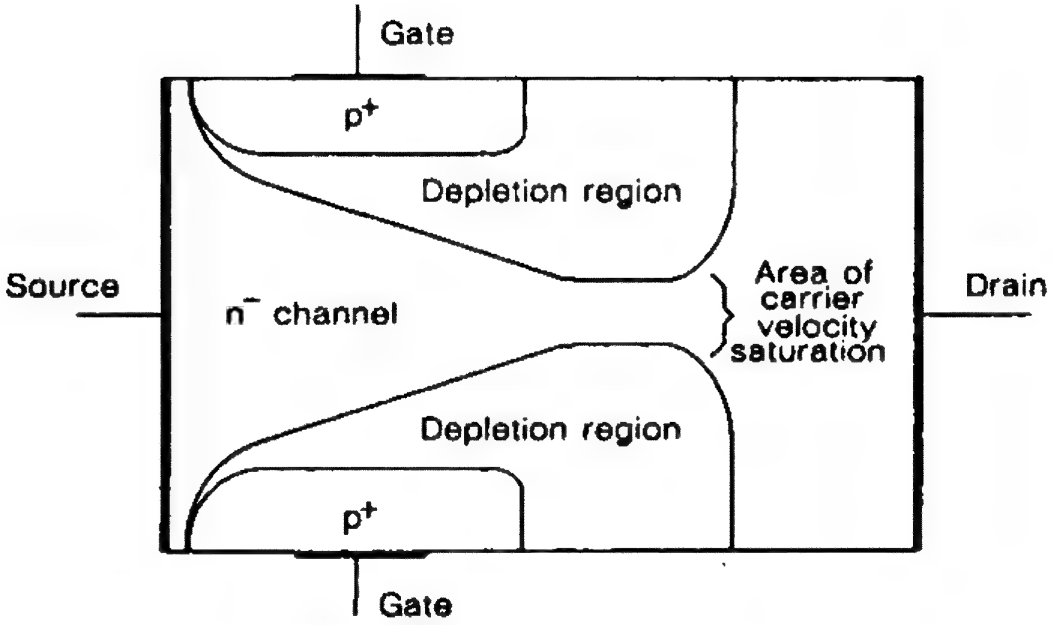


Figure 4.5 Shape of the conductive channel for a short-channel JFET. Because the channel restriction occurs beyond the gate area, we may see that $V_p \neq V_{GS(off)}$.

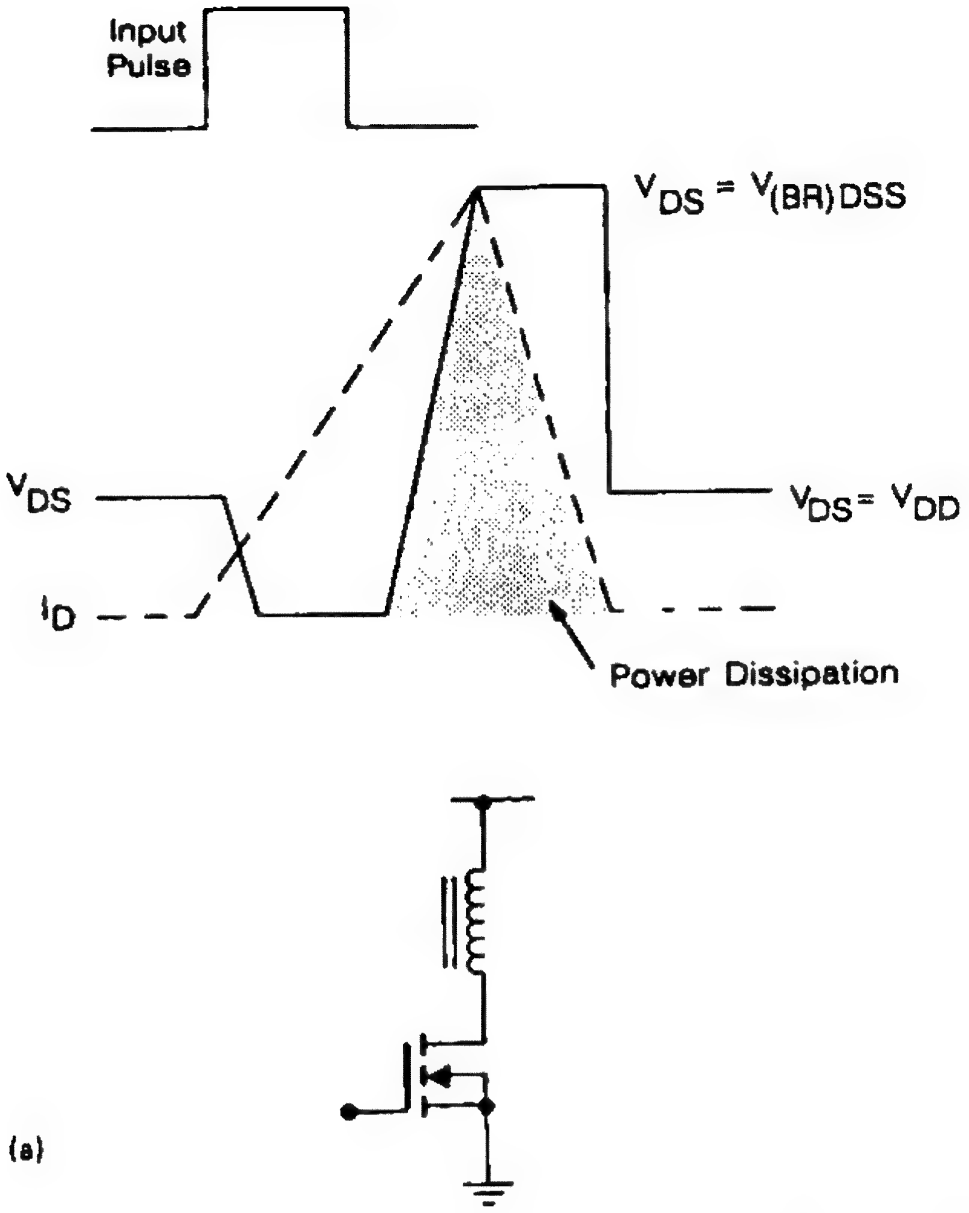


Figure 4.6 (a) Idealized waveform of an unclamped inductive load test. (b) The prime failure mode occurs when excessive current passing through the p^- region develops sufficient voltage across R_{p^-} (the p^- resistivity) to excite the parasitic npn transistor into conduction. If the drain voltage exceeds BV_{CEO} (of the npn), catastrophic breakdown may result.

upward beyond $V_{(BR)DSS}$, thus forcing avalanche current through the DMOSFET. The waveform is shown in Figure 4.6a. The cause of failure is easily understood by studying Figure 4.6b. The measurement may be done as a repetitive test.

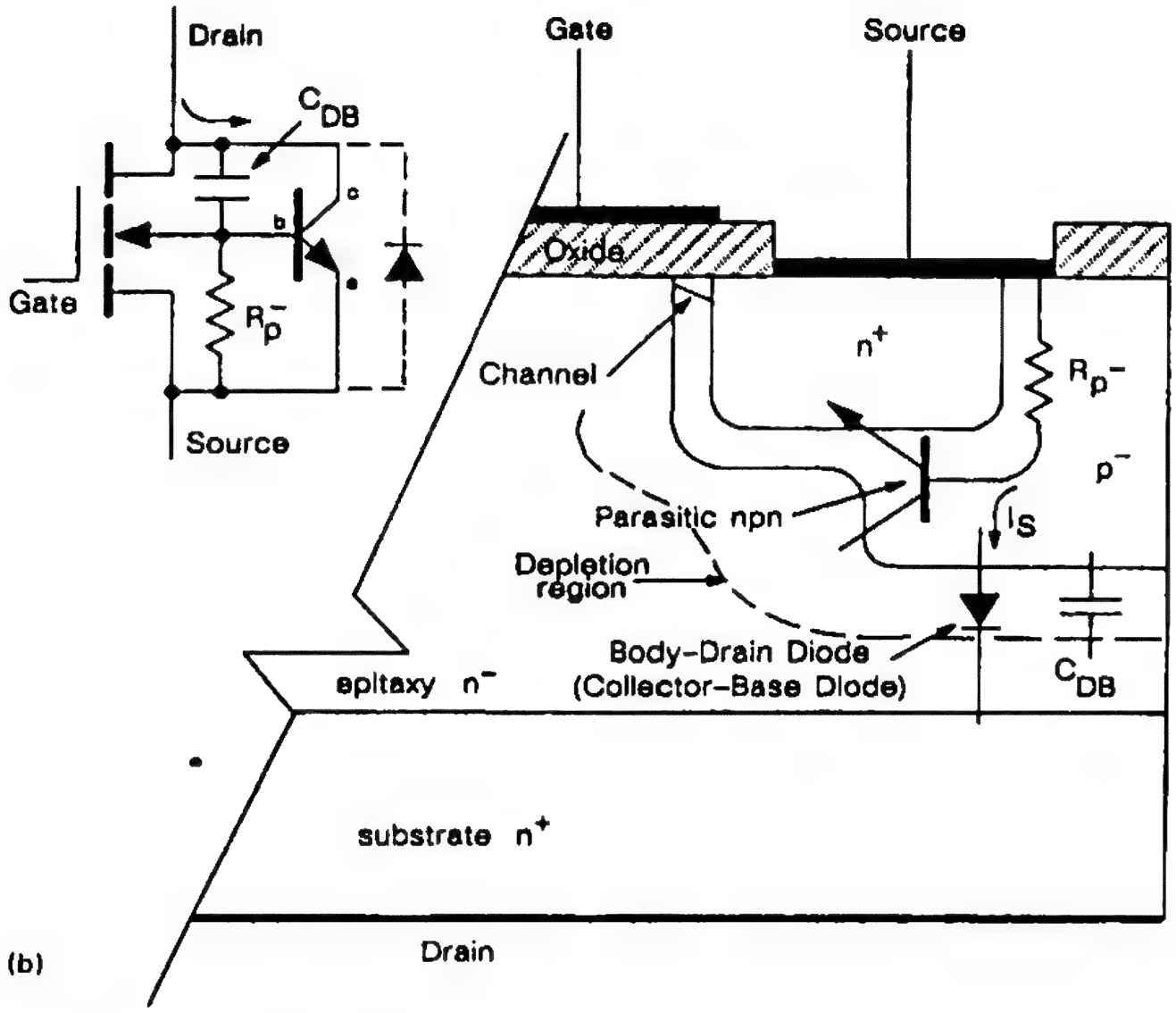


Figure 4.6 Continued.

4.2.9 I_D *Drain Current*

Small-Signal FETs

For both JFETs and MOSFETs, drain current is established simply by applying the properly polarized bias to the gate. As the bias is adjusted in magnitude, the resulting change in current is known as the *transfer characteristic*, dI_D/dV_{GS}.

DMOSFET

In Chapter 3 the drain current was identified as a *calculated* rather than a measured value. Rated drain current in a power DMOSFET is based on *dissipation* and ON resistance—Ohm's law.

A series of power DMOSFETs exhibiting identical ON resistance but differing in dissipative ratings will not offer the same current rating, *even if the active element is the same in all packages*. Equation 3.1 is used to calculate I_D.

Under the general heading of "absolute maximum ratings," where I_D appears on a data sheet, we occasionally find the current given in both polarities (±). This does not mean that the FET is bidirectional. It does imply that the semiconductor is capable of handling that level of current either through the FET channel or, if in the reverse direction, through the body-drain diode (see comments on I_S).

4.2.10 $I_{D(on)}$ *ON-State Drain Current*

Although I_D is generally rated with the absolute maximum ratings (at 25°C) on the power DMOSFET data sheet, $I_{D(on)}$ is always given as a *minimum* value on the same data sheet, even though these parameters are often (but not always) equal!

The fundamental difference between I_D and $I_{D(on)}$ is that the former is calculated, whereas the latter is measured. However, $I_{D(on)}$ is generally measured at a drain voltage sufficiently low (often at 2 times $V_{DS(on)}$, and under pulse conditions, to ensure that the maximum power dissipation of the power DMSOFET is not violated.

Optimizing $I_{D(on)}$ is the job of the semiconductor designer, and it involves a multiplicity of tasks. To raise this level of current, we must lower the resistivity as well as increase the active periphery of the source diffusion. Of course we have the options of increasing the size (active area) of the semiconductor chip or paralleling multiple chips. (Paralleling multiple chips in one header is not recommended, however, because experience, later confirmed by theory, identified a debilitating and often destructive oscillation occurring between DMOSFET chips mounted on a single header.)

4.2.11 $I_{D(off)}$ *Drain Cutoff Current*

The high ratio of OFF to ON resistance of the JFET makes this device popular in the market for large, solid-state analog switches. This specification is often found whenever JFETs are used as switches because it denotes the d-c OFF isolation when the JFET is biased beyond cutoff.

Shockley's power law equation for JFETs (Eq. 2.2), repeated here,

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4.2)$$

identifies the drain current falling to zero when V_{GS} equals $V_{GS(off)}$. In a practical sense this does not happen. It is true that the drain current I_D, drops to a very low value, but Eq. 4.2 does not consider the *leakage* current. As the value of V_{GS} approaches, then passes $V_{GS(off)}$, we see what we identify as $I_{D(off)}$—a drain-gate leakage current.

Of particular interest, not only do we witness a drain-gate leakage, but we also have a gate-source leakage current. If V_{GS} exceeds the reverse gate-source breakdown voltage (through indiscriminately increasing the bias well beyond $V_{GS(off)}$, we will discover an abrupt *increase* in $I_{D(off)}$! The effect is clearly shown in Figure 4.7.

It is because of this phenomenon that we assign a somewhat arbitrary drain current (always greater than $I_{D(off)}$) to identify $V_{GS(off)}$.

We need to be aware of one precaution, not just for $I_{D(off)}$ but for *all* leakage currents: a good rule of thumb is to assume that the leakage current doubles for every 10°C increase in chip temperature.

Leakage currents for low-voltage FETs closely obey the simple Shockley diode model that predicts

$$I = I_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \qquad (4.3)$$

where I_0, the reverse saturation current, also exhibits a temperature dependency:

$$I_0 = AT\ \exp\left(\frac{-1.12q}{2kT}\right) \qquad (4.4)$$

where

T = temperature in degrees Kelvin
q = electronic charge (1.602×10^{-19} C/electron)
k = Boltzmann's constant (1.38×10^{-23} J/°K)
A = a constant

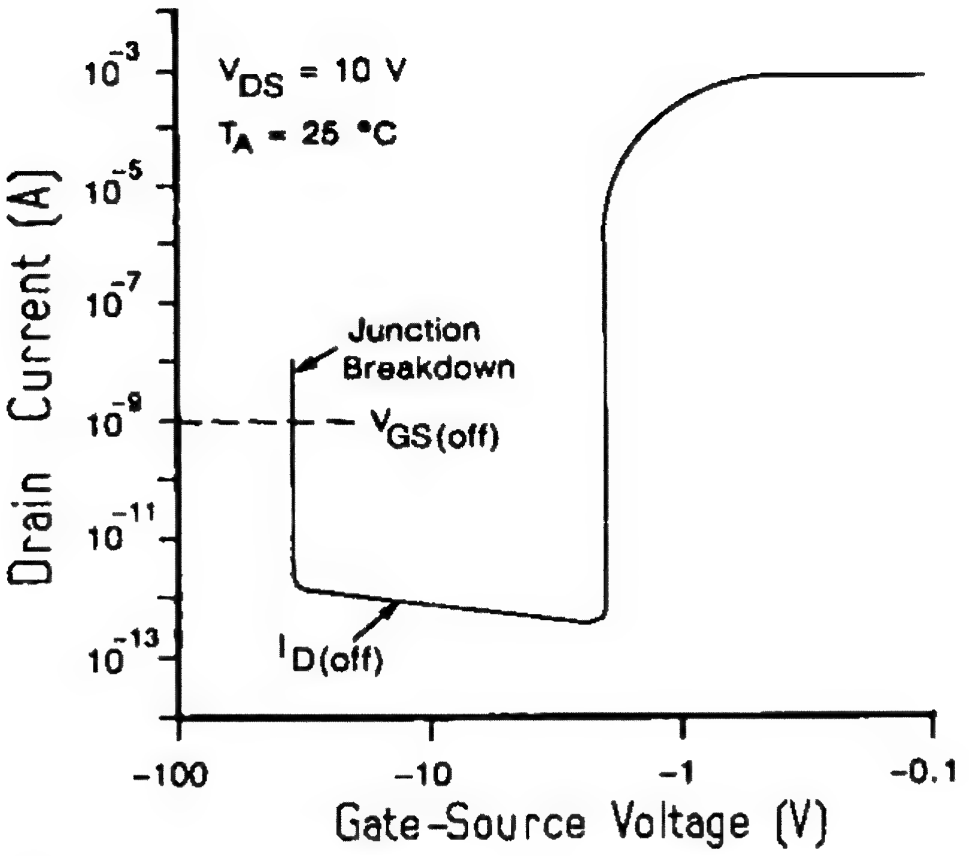


Figure 4.7 The effect of gate-source voltage on drain leakage current. (From *Designing with Field-Effect Transistors* by Siliconix inc., Arthur Evans, Ed. Copyright © 1981, McGraw-Hill Book Co. Used with permission.)

Equation 4.4 indicates that I_0 doubles for approximately every 10°C. The leakage current phenomenon becomes more complicated as the voltages rise. At voltages higher than what is generally expected with JFETs we find what is called a Hall-Shockley-Reed (HSR) effect. Although quite beyond the scope of this introductory text, the HSR effect comes from the natural imperfections that are symptomatic of any semiconductor (lattice) structure. Because of these imperfections, leakage currents find their way across pn junctions, adding their contribution to the leakage defined by Eq. 4.3.

4.2.12 I_{DM} *Pulsed Drain Current*

Do not assume that the specification for I_{DM} is related to the fusing current of the source bond wire. It seldom is! Unfortunately, the majority of power DMOSFET data sheets offer

no assurance other than that of providing this specification within the table of absolute maximum ratings (at 25°C)!

This specification *should* ensure the user that drain-current saturation has *not* been reached when operating the DMOSFET just shy of $V_{(BR)GSS}$. However, watch out for V_{SAT}—it may be higher than you at first imagine because of a phenomenon called the *pinch resistance*, which we discuss in Chapter 5.

4.2.13 I_{DSS} *Zero-Bias Drain Current*

Depletion-Mode JFET

The term I_{DSS}, is generally used to indicate the value of the saturated drain current at zero gate-source voltage (viz., when $V_{GS} = 0$). For a depletion-mode JFET, this term reflects a maximum drain current. Possibly a more accurate concept would identify I_{DSS} as the point of intersection where the triode and pentode output characteristics meet, at a drain voltage equal to V_p.

Depletion-Mode MOSFET

An unusual characteristic of the depletion-mode MOSFET is that once we have achieved a zero-biased drain current (I_{DSS}), we can continue raising our gate bias (passing the gate polarity through the zero crossing) and witness a drain current that exceeds I_{DSS}! Although the MOSFET is now operating in the enhancement region, we must remember that the term I_{DSS} exists only at zero bias. Any additional increase in the level of drain current I_D is *not* called I_{DSS}.

Enhancement Mode (MOSFET only)

With gate tied to source (the definition of I_{DSS}), an enhancement-mode MOSFET is normally OFF. Consequently this term reflects the *leakage* current between drain and source. Since enhancement-mode MOSFETs have no definable channel when in the OFF-bias condition, the common leakage path is diode leakage.

4.2.14 I_C *Operating Gate Current*

JFET operating gate current does *not* mean forward gate current. It always refers to the reverse current through the pn gate/channel junction when the JFET is biased for a specific drain current.

Although the gate/channel diffusion (pn junction) resembles a diode junction and, therefore, should seemingly offer similar characteristics, the fact that the JFET channel carries current dramatically alters its behavior.

Where the pn diode exhibits a rather well-understood reverse breakdown voltage characteristic, the pn (gate/channel) diode of the *operating* JFET does not. The latter effect is well behaved, but from a different point of view. Figure 4.8 plots gate current versus drain-gate voltage, showing clearly the remarkable difference between the expected pn breakdown voltage (I_{GSS}) and the operating breakdown voltage. Note the "I_G breakpoint" depends critically on *both* the operating drain current I_D, and the drain-gate voltage V_{DG} (*not* as V_{DS} as some data sheets erroneously state).

Since I_G is the result of collisions with silicon atoms in the gate region of highly excited free electrons (due to the drain-gate bias), as additional electrons (carriers) are introduced by operating the JFET, the collisions increase in frequency and the gate current increases in magnitude.

Gate current I_G, is a linear function of drain current I_D, and is exponentially related to V_{DG}.

4.2.15 I_{GSS} *Gate Reverse Current*

JFET

For any pn junction, whether a diode or a JFET, the reverse leakage current follows a well-behaved pattern, as shown in Figure 4.8. This current may arise from several causes, such as surface contamination or the diffusion of thermally generated hole-electron pairs (carriers) from the channel into the gate-depletion region.

Leakages tend to double for every 10°C increase in chip temperature (Eq. 4.3 and 4.4), and rise exponentially with increasing voltage, as shown in Figure 4.9.

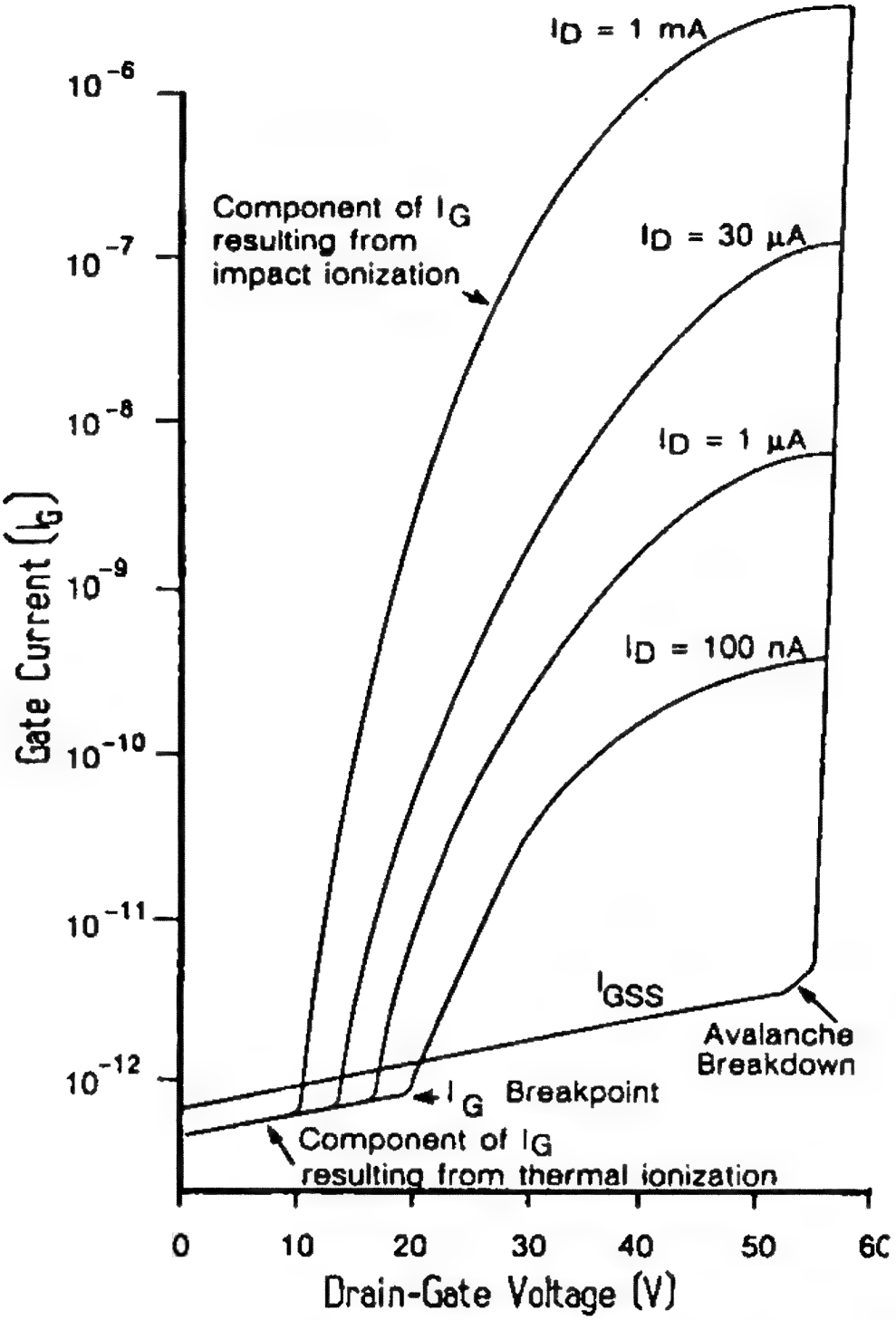


Figure 4.8 Effect of drain current and drain-gate voltage on operating gate current.

MOS

The principal cause of MOS-gate leakage is the presence of contaminants within the oxide interface between the gate and channel. These contaminants may be trapped electron charges or other surface-state events.

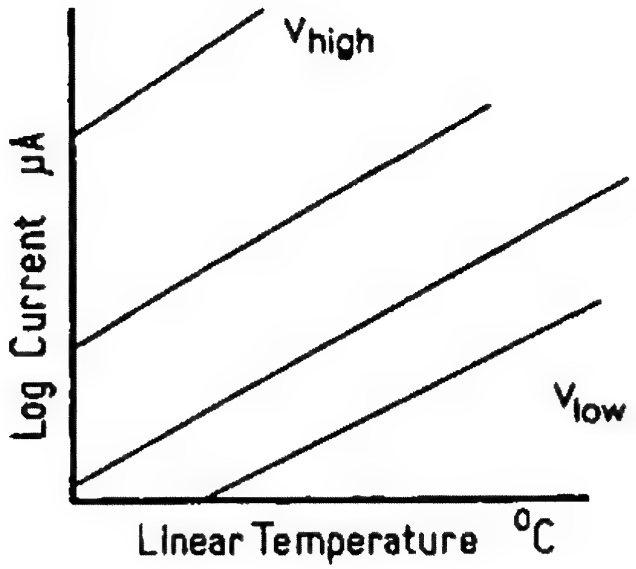


Figure 4.9 Leakage currents rise exponentially with the impressed voltage across the junction and double for each decade rise in temperature.

4.2.16 I_S *Source Current* [also I_{DR}— Continuous Reverse Drain Current]

It is critical to the success of the characterization of the power DMOSFET's body-drain diode to ensure a proper *forward* diode current. Because of the polarity of the body-drain diode (reverse that of the MOSFET itself), this diode current is forced into the *source* of the power DMOSFET (hence the alternate: I_{DR}, *reverse* drain current). The magnitude of this diode current is generally set by the manufacturer and should be equal or close to the calculated absolute maximum current (I_D) of the particular DMOSFET, at a temperature of 25°C.

Since reverse recovery time (see t_{rr}) depends critically on the magnitude of this current, we need to take special precautions to ensure that I_S is a *meaningful* value.

To gain an appreciation of the potential magnitude for I_S, we need only examine the periphery of the p-diffusion of an n-channel power DMOSFET, shown in Figure 1.18. The pn junction far exceeds the enhanced channel of the MOSFET, suggesting that I_S can well exceed I_D.

4.2.17 $r_{DS(on)}$ *Drain-Source ON Resistance*

Small-Signal JFET

In Chapter 1 we rather thoroughly examined channel conduction for the JFET and saw that the depletion width within the channel is proportional to the square root of the junction potential as defined by Eq. 1.1.

Channel conductance (and its reciprocal—$r_{DS(on)}$) is affected by several obvious factors: the cross-sectional area, the length, and the resistivity (doping concentration) of the channel, and, of course, the bias. The greater the cross-sectional area, the lower the resistance and the more heavily doped the channel—again, the lower the resistance. The longer the channel, the higher the channel resistance.

We exercise control over the channel resistance by the manipulation of the gate-source bias V_{GS}. At zero gate-source voltage we are very close to the optimum channel conductance (minimum resistance). When the gate-source voltage is extended beyond $V_{GS(off)}$, the channel conductance reaches its lowest value and the ON resistance of the JFET is nearly infinite. This is clearly illustrated in Figure 4.10, where r_{DS} versus V_{GS} normalized to $r_{DS(on)}$ and $V_{GS(off)}$ shows an exponential rise in ON resistance.

However, on the other hand, by careful manipulation of the gate bias (forward biasing, but *not* to where forward gate current commences), it is possible to further collapse the junction potential (V_{bi} of Eq. 1.1) and achieve additional reduction of channel resistance. We can see the results of such a manipulation in Figure 4.11.

Small-Signal MOSFET

As we saw with the small-signal JFET, channel conductance, hence resistance (the reciprocal of conductance), is affected by the channel area and length as well as by the dopant concentration.

For the depletion-mode MOSFET, the lowest channel resistance occurs when the gate bias has brought the MOSFET into enhancement. Once the gate bias has reversed its polarity (viz., matching the drain polarity), additional oppositely charged carriers are attracted to the region under the existing channel. As these oppositely charged (with respect to the gate charge)

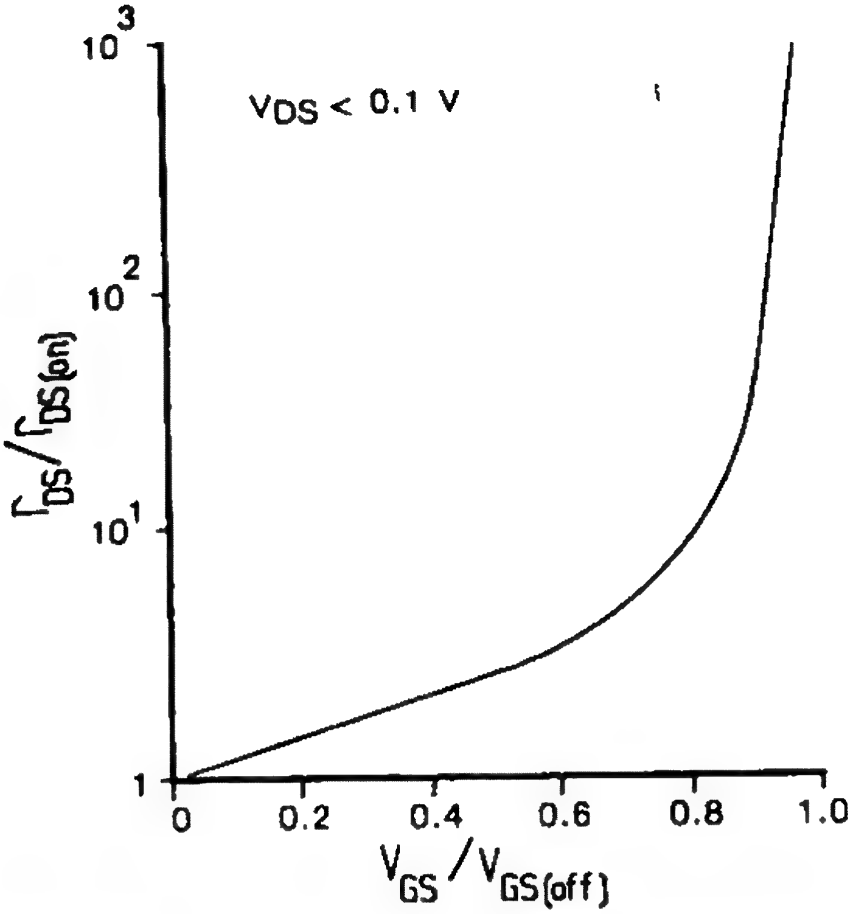


Figure 4.10 Normalized ON resistance versus normalized gate-source voltage.

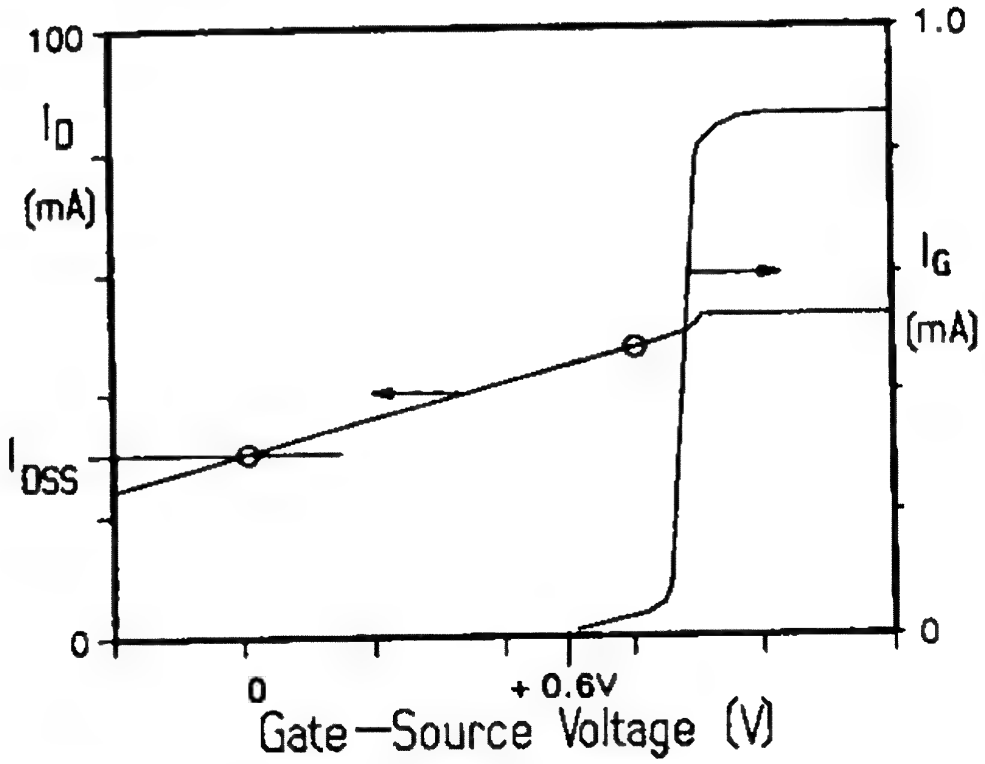


Figure 4.11 Effect of forward gate bias for a JFET showing a remarkable rise in the saturated drain voltage (Siliconix U310). Current saturation was purposely established to protect against burnout.

carriers build up, substrate inversion occurs, resulting in increased channel cross-sectional area and lower channel resistance.

For the enhancement-mode MOSFET, the lowest channel resistance occurs when the gate bias reaches just shy of its gate-source breakdown voltage.

SIT

Matters become complicated with the static-induction transistor because to obtain the desired triodelike output characteristics, we must optimize the channel thickness. Consequently a low $r_{DS(on)}$, although of prime importance, is somewhat compromised to provide the desired triode characteristic, and, simultaneously, reasonable efficiency.

DMOSFET (Power MOSFET)

The cost of a power DMOSFET (aside from any extra costs arising from special handling) is based principally on its physical size. Nothing more, nothing less. The number of good die per wafer eventually establishes the cost. Consequently, we strive for what might be an optimized design—optimized, that is, to offer the required breakdown voltage and ON resistance.

The ON resistance of power DMOSFETs with breakdown voltage in excess of 50 to 60 V is a function of the breakdown voltage, as we remember from Eq. 2.3, repeated here:

$$R_{DS(on)} = KV_{(BR)DSS}^{2.5} \tag{4.5}$$

where K is a proportionality constant reflective of the active area of the semiconductor chip.

For any given breakdown voltage, the larger the active area of the chip, the lower the ON resistance.

Fabricating a DMOSFET requires a compromise of sorts to achieve a high breakdown voltage and a low ON resistance. These properties do not complement each other. Either you increase the substrate resistivity to accommodate the required breakdown voltage, or you lower the substrate resistivity to reduce the ON resistance. The only alternative is to raise the resistivity to meet the breakdown requirements and increase the active area (or cell density) of the geometry to reduce the resistance.

Yet, we must be aware that there are subtle anomalies in merely increasing the *active* area of the semiconductor. Earlier in our discussion of $V_{(BR)DSS}$, we identified several design concepts for improving the breakdown voltage capability of the semiconductor. All these concepts to improve performance require some finite area. Likewise we need bonding pads where source and gate contact is made. Consequently, the *physical* area of a power semiconductor chip is greatly exaggerated when compared to the *active* area.

To achieve cost-effective solutions, bonding over active area is replacing the source bonding pad. Most, if not all power DMOSFET design has source metal across the face of the semiconductor die (chip), providing ample bonding area without the need of a special bonding pad. This affords some improvement in surface utilization.

Additionally, in the initial design of the semiconductor chip we must chose our layout carefully. To achieve an optimum design, manufacturers may chose from several topologies, some of which are shown in Figure 4.12.

4.2.18 $r_{ds(on)}$ *Dynamic ON Resistance*

We measure by modulating the gate voltage V_{GS} and measuring both the a-c drain voltage and a-c drain current, obtaining:

$$r_{ds(on)} = \frac{dv_{ds}}{di_{ds}} \tag{4.6}$$

4.2.19 R_{thJC} *Thermal Resistance, Junction to Case*

For a given semiconductor chip size, R_{thJC} depends on two design decisions:

1. The means by which the chip is bonding to the case (the die attach), such as by gold eutectic, soft solder, or epoxy.
2. The package (case), both in composition (copper, steel, aluminum, etc.) and in physical size. A copper TO-204 package will offer a lower thermal resistance than a steel TO-204, and both will offer a lower thermal resistance than a copper TO-205.

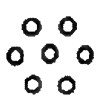
Square on Square Grid	Circle on Square Grid	Hexagon on Square Grid	Square on Hexagon Grid	Circle on Hexagon Grid	Hexagon on Hexagon Grid
					
					
1.0	.886	.931	1.07	.952	1.0

Figure 4.12 Efficiency of various DMOSFET surface geometries. Note that the "square on hexagonal grid" form is the most efficient.

4.2.20 R_{thCS} *Thermal Resistance, Case to Sink*

The value of R_{thCS} is also determined by two design decisions, but these decisions are the responsibility *not* of the vendor but of the *user*! The user's decisions involve the package style chosen for the job, and, if the chosen package style allows attachment to a heatsink, the means used to attach the package to the heatsink.

4.2.21 R_{thJA} *Thermal Resistance, Junction to Ambient*

This resistance combines not only the sum of R_{thJC} *and* R_{thCS}, but also depends upon the *user's* choice of heatsink and cooling.

4.2.22 g_{fs} *Forward Transconductance*

A measurable quality of a FET's performance as defined by its gain may be expressed by the following relation:

$$g_{fs} = \frac{dI_D}{dV_{GS}} \quad [V_{DS} \text{ a constant}] \qquad (4.7)$$

JFET

If we differentiate Shockley's equation (Eq. 2.2, repeated as Eq. 4.2), we arrive at the small-signal transconductance:

$$g_{fs} = \frac{-nI_{DSS}}{V_{GS(off)}}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^{n-1} \tag{4.8}$$

where n is generally 2, although some texts identify a variance ranging between 1.5 to 2.5.

If $V_{GS} = 0$, then Eq. 4.8 reduces (with n = 2) to:

$$g_{fs} = \frac{-2I_{DSS}}{V_{GS(off)}} \tag{4.9}$$

leading us to understand that the small-signal transconductance of a JFET is proportional to the saturation drain current and inversely proportional to the gate cutoff voltage.

Equation 4.9 also indirectly identifies a relationship between I_D and g_{fs}, best shown in Figure 4.13.

MOSFET (Small Signal)

The basic equation (Eq. 4.7) holds equally well for any FET, JFET or otherwise. In Section 2.3 we learned that the MOSFET has a fourth terminal, the substrate. One precaution we need to be aware of is that this substrate can act as a pseudo-gate. As a consequence, when we consider transconductance, we need to determine whether we are considering *gate* transconductance or *substrate* transconductance. In both cases, the basic equation holds; what differs is the denominator: Is it dV_{GS} or dV_{BS}? The term V_{BS} identifies the body (or substrate)-to-source voltage. Every effort is usually taken to reduce the latter and enhance the former, often by the simple expedient of tying the substrate to the source.

There are several variables to optimize MOS transconductance, evident in Eq. 4.10:

$$g_{fs} = \frac{C_{ox}\,\mu_n\,W(V_{GS} - V_T)}{L} \tag{4.10}$$

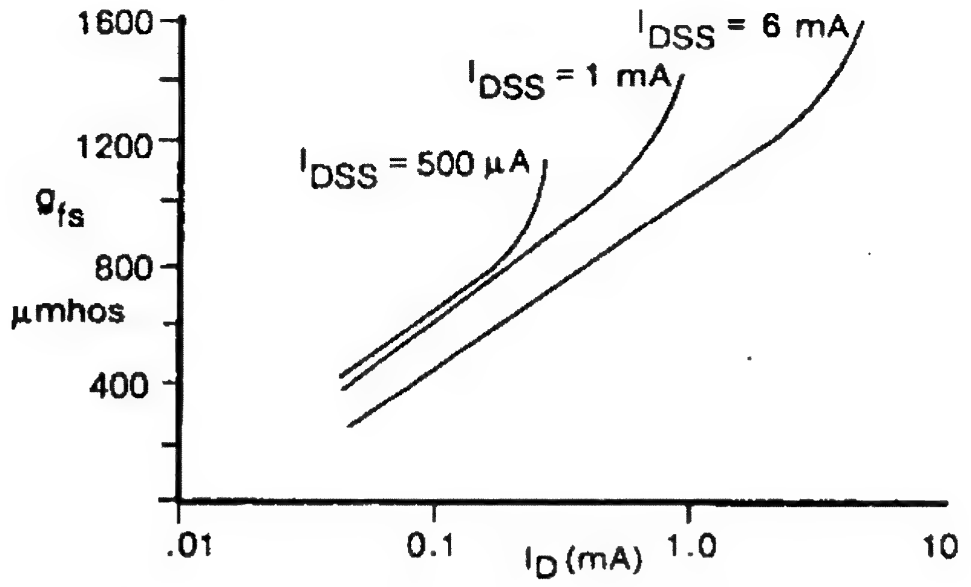


Figure 4.13 Graphical representation of Eq. 4.9 as applied to the JFET.

where

C_{ox} = gate oxide capacitance per unit area
μ_n = electron mobility in the n-region
W = width of the channel
L = drain-source separation (channel length)

Close inspection of Eq. 4.10 suggests that transconductance may be increased by increasing either V_{GS} or decreasing V_T. Unfortunately, the drain current will increase as the square of $(V_{GS} - V_T)$, making power dissipation unduly severe.

SIT

Because the static-induction transistor does not follow the classic Shockley equation (Eq. 2.2), a clear understanding of its transconductance is difficult. One complexity results from the SIT's nonsaturating drain current dependency on drain votlage (see Figure 2.7).

To even approach a phenomenological understanding of transconductance, in light of Eq. 4.7, we must resolve the effects of *drain voltage* on drain current. However, complicating matters further, the SIT appears to alter its I_D/V_{DS} relationship as we move from the low-current to the high-current state.

Since the SIT behaves much like the classic triode, we can approach a phenomenological understanding of transconductance

if we recognize that the relative effectiveness of the drain and gate potentials is, in reality, nothing more than the *amplification factor*, μ!

$$\mu = -\frac{dV_{DS}}{dV_{GS}} \quad \text{at } I_D = \text{constant} \tag{4.11}$$

Observation of the SIT output characteristics (Figure 2.7) shows that the curves are similar, only displaced from one another. This is partly because the drain current depends on *both* V_{GS} and V_{DS}, as we see in the following equation:

$$I_D = \frac{V_{DS}}{(1 + \mu)r_s} + \frac{\mu V_{GS}}{(1 + \mu)r_s} \tag{4.12}$$

where

μ = amplification factor (Eq. 4.11)
r_s = resistance between the source and the intrinsic gate

To determine the transconductance of the SIT, we need to establish a *load line*. The load line (superimposed on Figure 2.7) in Figure 4.14, identifies the dynamic drain-load impedance, as follows:

$$R_d = \frac{dV_{DS}}{dI_D} \quad [V_{GS} \text{ a constant}] \tag{4.13}$$

Merging Eqs. 4.7 and 4.13, we discover that transconductance is numerically equal to:

$$g_{fs} = \frac{\mu}{R_d} \tag{4.14}$$

It is interesting to note that with JFETs, the voltage gain (or μ) is equal to the product of transconductance g_{fs}, and the load resistance R_d. Not really different from the SIT!

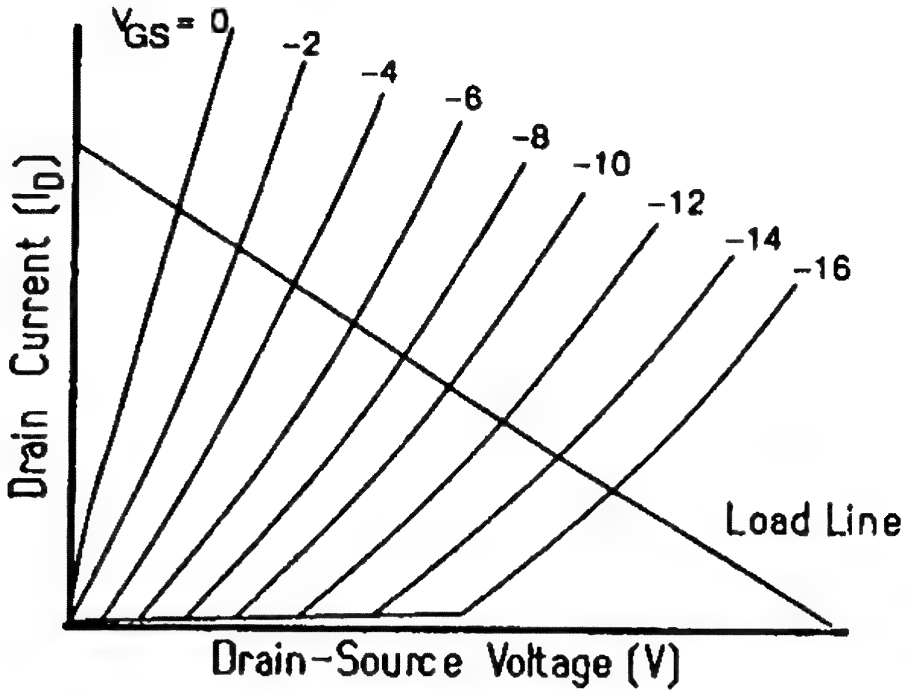


Figure 4.14 Typical output characteristics of the SIT with load line superimposed.

DMOSFET

The power DMOSFET likewise exhibits a change in state as the drain current rises. What is especially remarkable results from the short channel length inherent in all DMOSFET structures. At sufficiently high electric fields, carrier velocity saturates, at which point the gate bias no longer plays a part in determining the transconductance! At low currents the power DMOSFET operates essentially in the square-law region, and the equation for transconductance is:

$$g_{fs} = \frac{\mu_n C_{ox} W (V_{GS} - V_T)}{L} \qquad (4.15)$$

When velocity saturation occurs, the equation becomes:

$$g_{fs} = \frac{C_{ox} W E}{2} \qquad (4.16)$$

where E is 5×10^6 cm/s for silicon.

Note that the term in parentheses in Eq. 4.15 is no longer applicable. The one readily controllable variable, W, suggests

that as our die size increase (to accomodate higher currents), so does the transconductance.

IGBT

Equation 4.7 applies only to FETs; the IGBT, although possessing a gate really is not a true FET in every sense. A more realistic equation would be:

$$g_m = \frac{dI_C}{dV_{GE}} \tag{4.17}$$

where

I_C = collector current
V_{GE} = voltage from gate to emitter

Because the IGBT is controlled by a gate potential rather than by the injection of minority carriers via the gate (but by minority carriers from the MOS channel), we use the term *transconductance* rather than the more familiar bipolar term, *beta*.

The term g_{fs} really means the forward transconductance with reference to a common source (common to both input and output). However, as we have just witnessed in Eq. 4.17, the IGBT does not have a source but an emitter, so the equally common symbol for transconductance, g_m, is used.

We need to be aware that an IGBT will find its principal application in high-level switching rather than as an amplifier; thus there is little need to know its transconductance.

4.2.23 g_{os} *Output Conductance*

Although a perfectly useful term, g_{os} is generally relegated to the characterization of small-signal JFETs and constant-current diodes made from JFETs.

Drain-current saturation as defined for a JFET (by I_{DSS}) can be confusing when we view the typical drain characteristics (Figure 2.2). Beyond the point of supposed drain-current saturation, I_{DSS}, we continue to see small increases in drain current with increases in drain voltage.

The effect becomes most apparent for short-channel JFETs, where the depletion region is affected not only by the gate potential but by the drain as well. For some short-channel JFETs (as well as DMOSFETs) this effect may be caused by velocity saturation, which produces a premature drain-current saturation that continues to be influenced by increasing drain voltage.

4.2.24 C_{iss} *Common-Source Input Capacitance*

Gate-source and gate-drain capacitance, as identified in Eq. 3.4, combine to form C_{iss}.

FETs with potential barriers established by carrier-free depletion regions have associated with them what we may label an *active* capacitance (later this will be shown to be distinct from a passive, or parasitic capacitance). The plates of this capacitor are the electric fields beyond the depletion region; the dielectric is the depletion region. Factors affecting the magnitude of capacitance involve the junction area, the doping concentration, and the applied voltage as well as its polarity. As the reverse bias voltage increases, the depletion region expands and reduces the capacitance. This can be visualized easily by studying how the depletion fields in a JFET are enlarged by the applied voltage, as shown in Figure 2.1.

Additionally, we have capacitances formed by layout—for example, the proximity of the gate to surrounding source metal. This we label as passive or *parasitic* capacitance.

Because FET capacitance is principally a phenomenon dependent on depletion fields and layout, we see few effects resulting from temperature.

Manufacturers often do not offer either C_{gs} or C_{gd}, but provide the JEDEC-approved *input* capacitance C_{iss}, in a common-source configuration (source common to both the input and output). Consequently, if we examine the plot of C_{iss} versus V_{GS}, shown in Figure 4.15, it is not difficult to be misled regarding the effects of voltage on input capacitance. Extracting the terminal capacitances using Eq. 3.4 and plotting as we have done (Figure 4.16) offers a succinct appreciation of the effects of voltage on gate source capacitance for the JFET.

Input capacitance, C_{in}, may, under certain conditions, differ from either C_{gs} or C_{iss}, when the *Miller effect* comes into play (see Section 4.2.28).

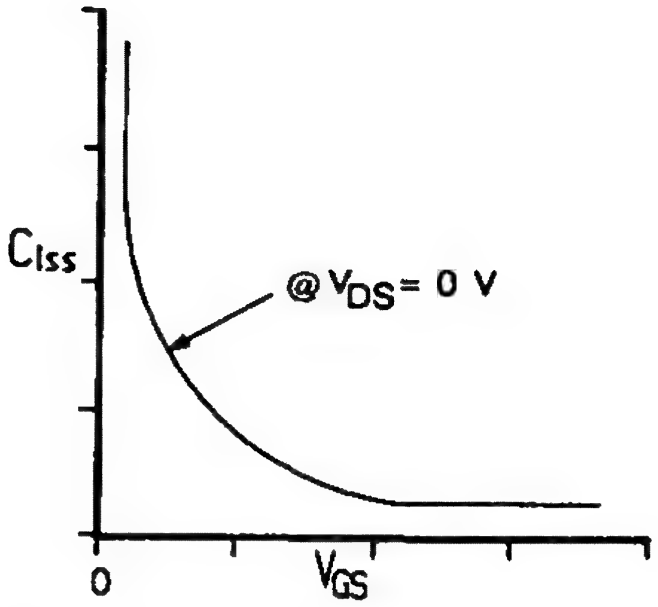


Figure 4.15 A linear plot of the common-source input capacitance C_{iss}, of a JFET as a function of gate-source voltage.

JFET

From Poisson's equation, the reverse bias space-charge capacitance per unit area of an abrupt-junction diode is an inverse function of the square root of the junction voltage:

$$C = \left(\frac{K}{V_{bi} + V_G}\right)^{1/2} \qquad (4.18)$$

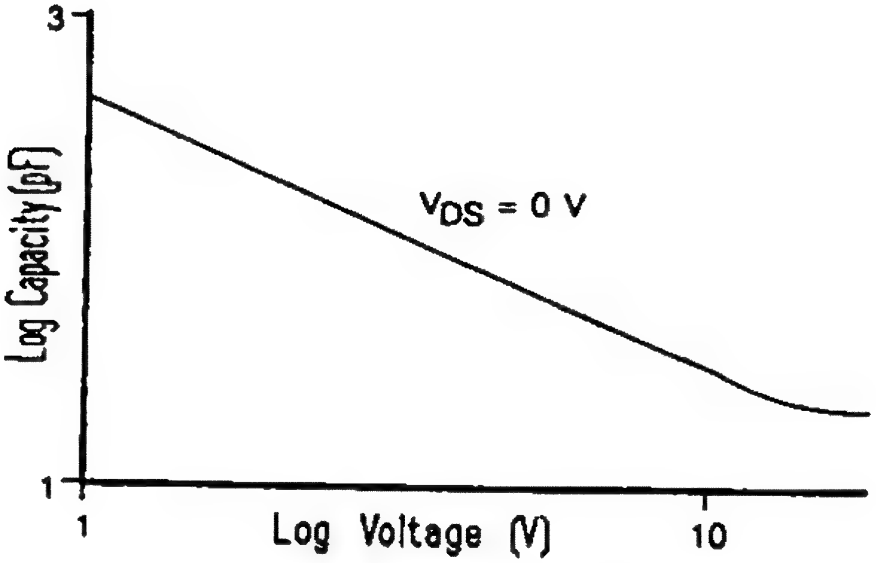


Figure 4.16 Gate-source capacitance C_{GS}, of a JFET versus gate-source voltage.

JFETs, as a rule, are not classified as abrupt-junction devices, for the diffusion processes will cause some gradation of the junctions. To modify Eq. 4.18 to better fit the JFET, we would change the exponent from 1/2 to 1/3.

If we carefully consider the cross-sectional view of a JFET (Figure 2.1), we will understand why gate-drain capacitance C_{gd}, is less than gate-source capacitance C_{gs}, even though the JFET is manufactured in perfect physical symmetry and source and drain may be interchanged in operation.

This effect becomes even more pronounced for planar short-channel JFETs, where we see very low values of C_{gd} due, in great measure, to the high electric fields present at the drain end of the channel. Because of their extremely low values of C_{gd}, such JFETs find wide application at high frequencies.

MOS and DMOS (Small Signal)

MOSFET capacitances are also affected by depletion-region movement in addition to other, more complicated, factors. One of these complications results from trapped charges resident in the gate oxide.

The equation for the MOS capacitor is:

$$C_{ox} = \frac{e_{ox} E_{ox} A}{x_{ox}} \qquad (4.19)$$

where

e_{ox} = dielectric constant of the oxide
E_{ox} = electric field within the gate oxide
x_{ox} = thickness of the gate oxide
A = effective area of one plate

Charging the MOS Capacitor

Let us examine what happens when a charge is placed on one plate of a capacitor. Using Figure 1.7 as our model, we observe that for every positive charge we have a negative charge supplied by the mobile electrons in the p-substrate. Figure 4.17 is informative in that we see the effect of resident charges that permanently exist in semiconductor MOS dielectrics (identified in Eq. 4.19 as E_{ox}). When our gate voltage V_G, is in-

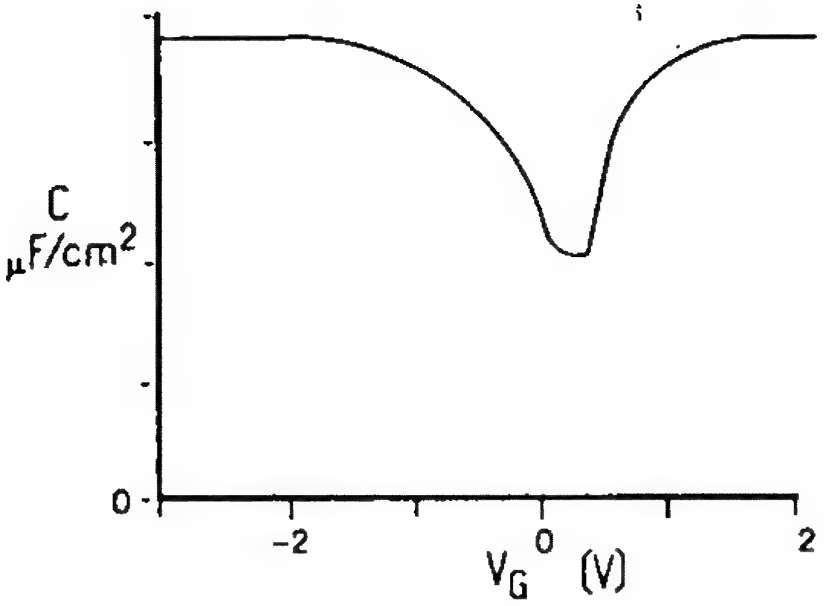


Figure 4.17 The effect of gate voltage on capacity of a small-signal MOSFET. The dramatic dip in capacity occurs as a result of the movement of the depletion region within the body, whereas the return to the former state (at positive bias) is caused by the development of an inversion layer immediately beneath the oxide (see Figure 1.7).

sufficient to overcome this resident charge, we see the capacitance take a sudden drop.

In our earlier discussion of $V_{GS(th)}$ for the enhancement-mode MOSFET, we learned that an additional gate bias was required simply to overcome the effects of this charge. In practice, the voltage within the gate oxide, V_{ox}, will differ from the applied gate-substrate (body) voltage, V_{GB}, simply because of the charge resident in the gate oxide. A simplified equation of the gate-substrate capacitance per unit area is:

$$C = \frac{C_{ox} \cdot V_{ox}}{dV_{GB}} \qquad (4.20)$$

The gate-source capacity C_{gs}, and gate-drain capacity C_{gd}, (which together equal C_{iss}) experience a dramatic increase when the gate bias V_{GS}, passes the threshold voltage V_T, as illustrated in Figure 4.18. We can credit this dramatic increase in capacitance to the carriers in the now-enhanced MOS channel which, with the gate, form the plates of a capacitor (Figure 1.7).

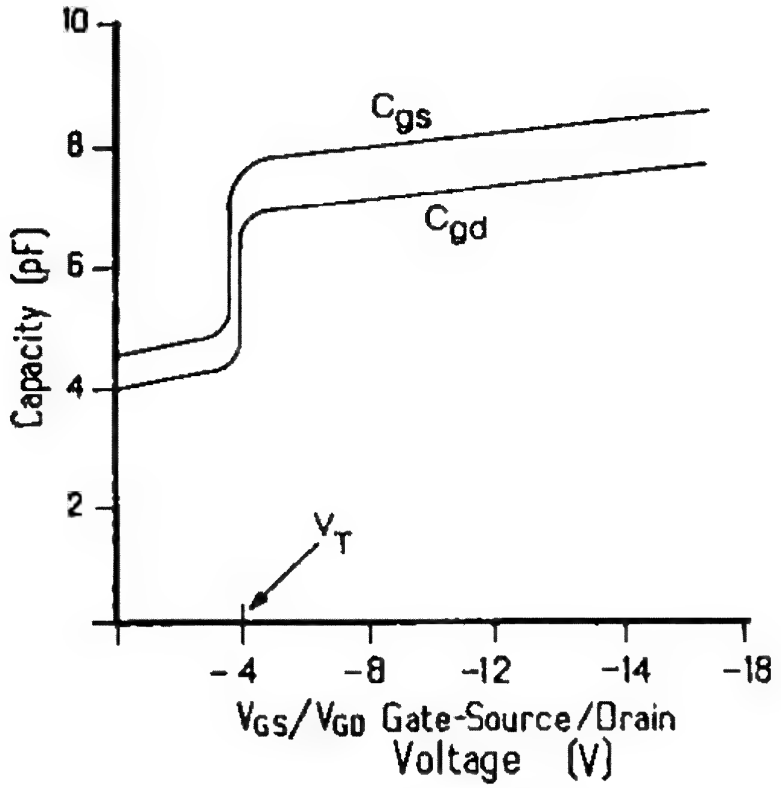


Figure 4.18 Effect of gate bias on capacity for a small-signal, enhancement-mode, n-channel MOSFET.

DMOSFET (Power)

Many of the effects we have just read regarding small-signal MOS also hold for power DMOSFETs. Again, the JEDEC format for itemizing capacitances lists C_{iss}, C_{oss}, and C_{rss}, which, when plotted, can lead to some confusion. Following our previous example, from Eq. 3.4, we can plot C_{gs} and C_{gd}, shown in Figure 4.19 for a 400 V, 1 Ω power DMOSFET. Notice that unlike the small-signal JFET or MOSFET, the gate-source capacitance C_{gs}, remains fixed as the drain voltage V_{DS} rises. This would not be immediately apparent if the reader were to check the effects of C_{iss} versus V_{DS}. Note also that V_{GS} is *below* threshold. Why C_{gs} remains fixed can be understood by a careful study of the power MOSFET cross-section in Figure 1.18. The power DMOSFET is *inoperable*. Once channel current has commenced our understanding of the effects on capacitance is further complicated. This has led JEDEC to recommend that *charge* data be offered on the data sheet (see Charge) in lieu of capacitance.

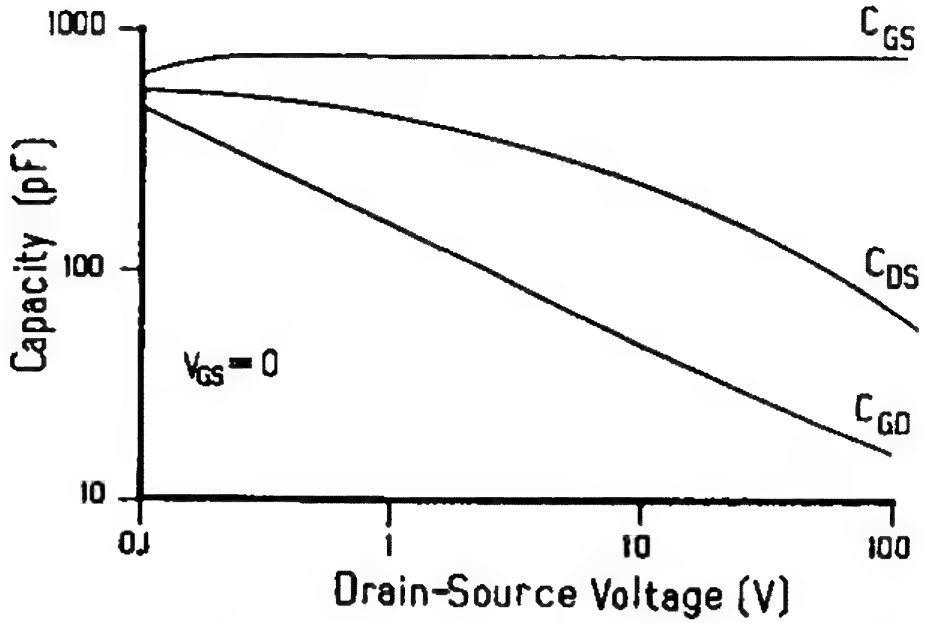


Figure 4.19 Interelectrode capacitances of a power DMOSFET versus drain-source voltage of a low-C_{gd}, 400 V, 1 Ω power DMOSFET. Here, we are able to resolve the true effect of voltage on the depletion-dependent capacitances.

SIT

Gate-source capacitance, C_{gs}, like the JFET, is depletion dependent. As bias is applied to the recessed gate (see Figure 1.15), the depletion field spreads quickly to assume a fully depleted region at moderately low bias voltage. Likewise the gate-source capacitance decreases rapidly, then gradually becomes marginally constant as shown in Figure 4.20.

IGBT

Ostensibly comparable to the power DMOSFET insofar as its gate input is concerned, nonetheless, the symbol probably should be C_{ge}—capacitance, gate-emitter. Like the power DMOSFET, C_{ge} should remain constant over wide "collector" voltages.

4.2.25 C_{oss} *Output Capacitance*

According to the JEDEC standards C_{oss} contains both C_{ds} and C_{dg} (see Eq. 3.5).

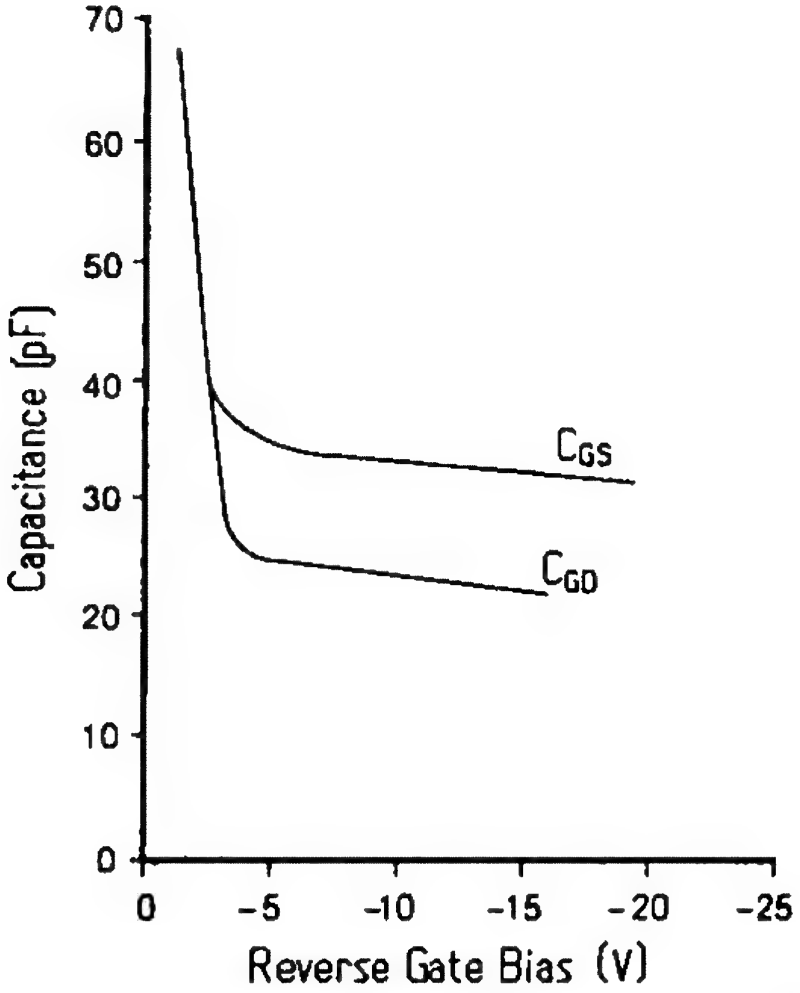


Figure 4.20 Effect of gate bias on capacitance in the SIT. The abrupt drop occurs as V_{GS} passes $V_{GS(off)}$. (From B. J. Baliga, "High Voltage Junction-Gate Field-Effect Transistor with Recessed Gates," *IEEE Transactions on Electron Devices*, ED-29. Copyright © 1982, IEEE. Used with permission.)

JFET

The drain-source capacitance C_{ds}, for the JFET is quite low, often so low that aside from high-frequency applications, and in switching fast pulses or high frequencies (analog switches), we can ignore it. We should, by now, recognize why C_{ds} is low. Capacitances are controlled by depletion fields; the depletion field established by the drain-source potential is of major proportions (as compared to all others), resulting in a very low capacitance. It would not be uncommon to see values in the high femtofarads (1 fF = 10^{-15} F). In fact, package parasitic capacitances will generally mask those of the semiconductor.

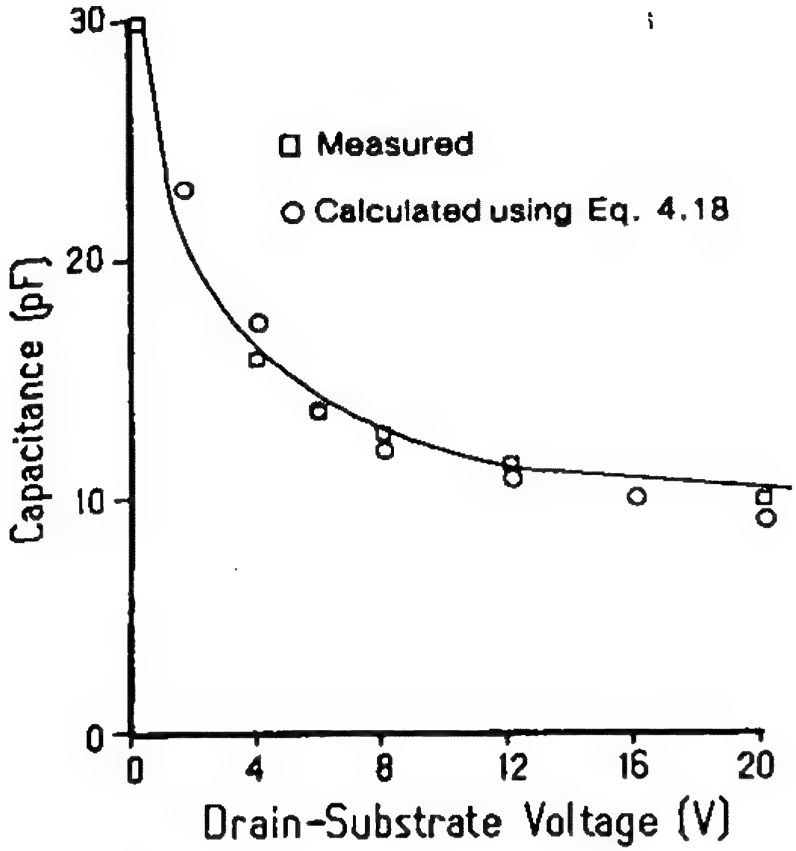


Figure 4.21 A comparison of measured and calculated values of drain-body capacitance of a small-signal, n-channel MOSFET.

MOS (Small Signal)

Output capacitance C_{ds}, consists primarily of the drain-body capacitance C_{db}, and, as such, more closely follows Eq. 4.18 (V_{DS} substituted for V_G). Consequently, we see that for the small-signal MOSFET, when V_{DS} is much greater than V_{bi}, C_{db} is inversely proportional to the square root of drain voltage. A comparison of measured versus calculated values (using Eq. 4.18) is offered in Figure 4.21 (shown in the OFF state).

DMOSFET

The classic cross-sectional view of the power DMOSFET shown in Figure 4.22 provides detailed information about the active and parasitic capacitances. As we may have suspected, the drain-source capacitance is, in reality, the drain-body capacitance. Earlier we affirmed that the power DMOSFET body is electrically bridged to the source, thus $C_{db} = C_{ds}$. Since C_{db} (hence C_{ds}) is a junction-depletion capacitance, we may also expect the capacitance to be inversely proportional to the square

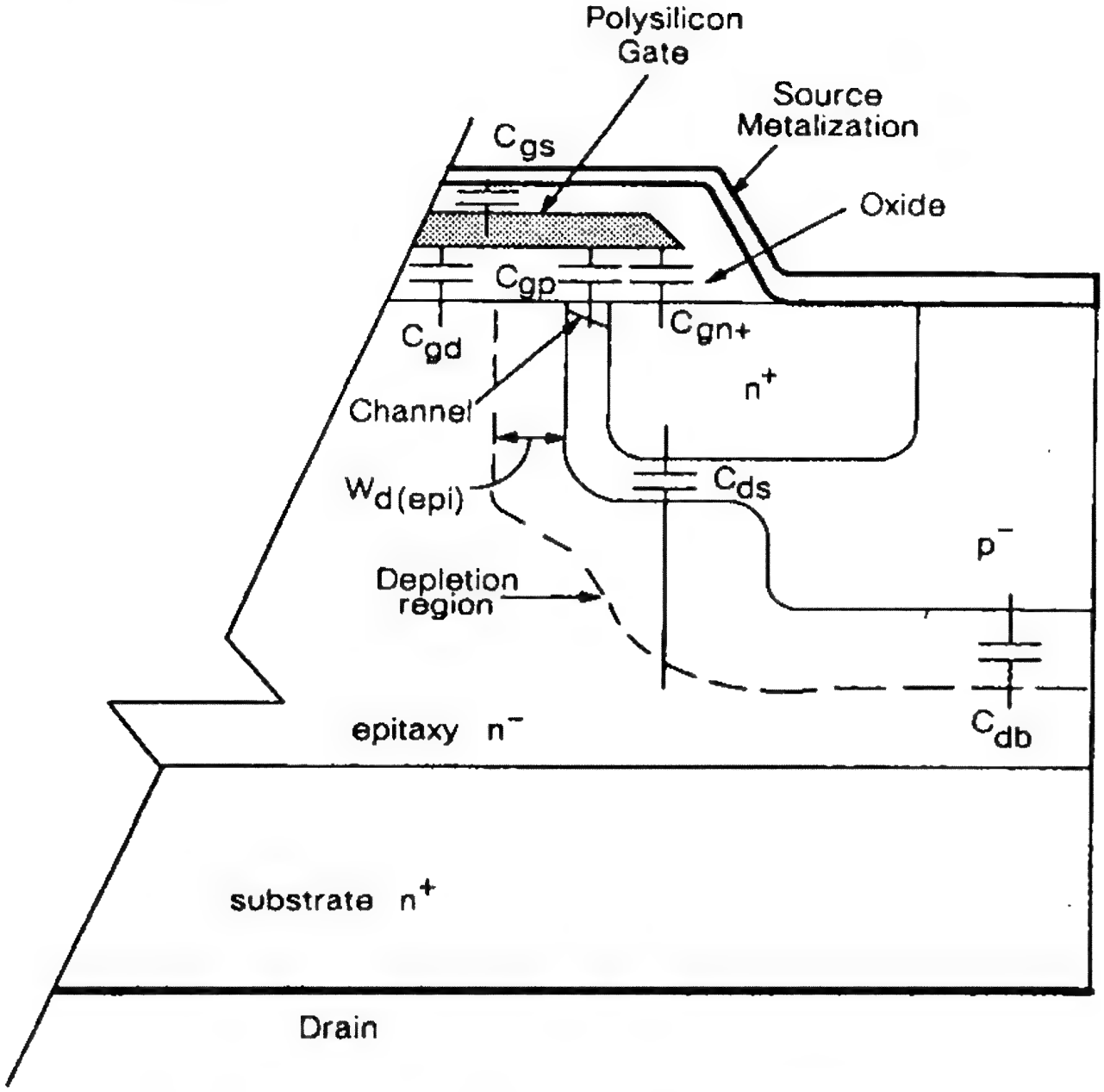


Figure 4.22 The location of parasitic capacitances in a power DMOSFET. Both gate-to-source (C_{gs}) and gate-to-n^+ (C_{gn+}) capacitances are essentially independent of bias voltages, whereas drain-body capacitance (C_{db}) and drain-source capacitance (C_{ds}) depend heavily on the depletion field, hence on the voltage.

root of the drain voltage (when $V_{DS} >> V_{bi}$). See Figure 4.19.

SIT

Unlike anything we have studied before—and what we can confirm by inspection of Figure 1.15, the output capacitance appears to be synonymous to the *feedback* capacitance, or drain-

gate capacitance C_{gd}! As we earlier witnessed with C_{gs}, we also see for C_{gd} (Figure 4.20).

IGBT

In the IGBT case, we are no longer dealing with a FET when we consider the output capacitance. Aside from its gate input, the IGBT is a power *bipolar* transistor. Like bipolar transistors, C_{ob}—output capacitance—remains reasonably constant regardless of collector voltage.

In the applications involving IGBTs, C_{ob} is not important. What is of paramount importance is *storage time* (see discussion on $t_{d(off)}$).

4.2.26 C_{rss} *Reverse Transfer Capacitance*

The reverse transfer capacitance is better recognized as C_{gd}—gate-drain capacitance, or feedback capacitance. No parasitic capacitance is desirable, and C_{rss} is the least desirable of all.

JFET

We know that all JFET capacitances are depletion-dependent, hence voltage-dependent. Where we have the greatest electrostatic differences, we shall see the lowest capacity. Even though most JFETs are fabricated with symmetrical cross-sections, because of the higher drain potential, we find the gate-drain capacity lower than gate-source capacity.

Yet a more subtle cause of feedback capacity, other than that caused by voltage-dependent depletion regions, might escape the casual reader.

There are two common topologies for JFETs (not including monolithic duals): the symmetrical and the asymmetrical, shown in Figure 4.23. The majority of JFETs today are fabricated on an epitaxial layer that forms a back gate. To provide electrical continuity between the top gate and the epi gate, a deep well extends through the semiconductor about the periphery of the chip, illustrated in Figure 4.24. The asymmetrical topology, in essence, envelopes the drain fingers with source fingers that effectively shield the drain from this deep gate well, which surrounds the periphery of the active area.

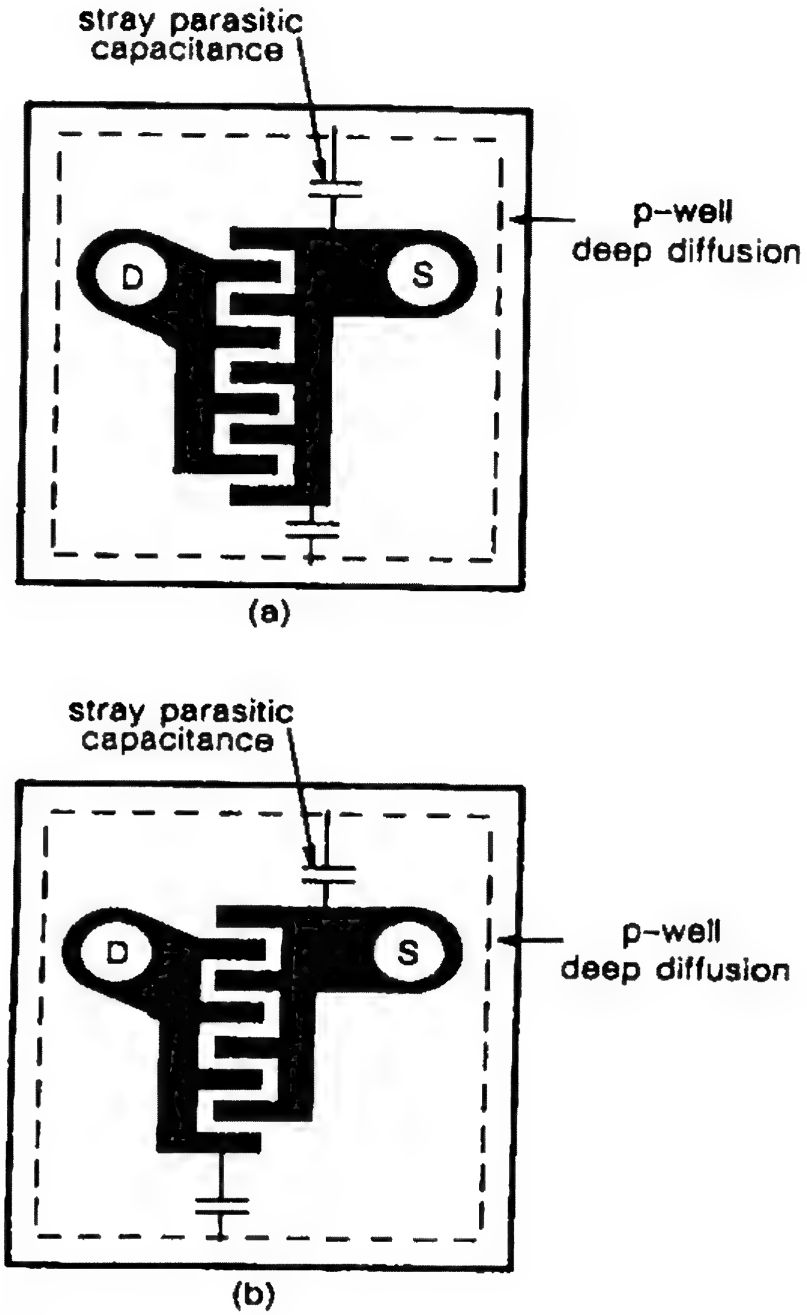


Figure 4.23 Asymmetrical (a) and symmetrical (b) JFET topology. The asymmetrical source fingers surround the drain fingers, reducing the parasitic drain-gate capacity. A slight improvement in the gain bandwidth occurs when operating at high frequencies (> 100 MHz).

MOS and DMOS (Small Signal)

Like the JFET, the small-signal MOSFET has a subtle contributor to feedback capacitance. In the design and fabrication of a MOSFET, to ensure carrier conduction between source and drain for an enhancement-mode device, the gate alignment with both source and drain diffusions must be precise (see Figure 1.8).

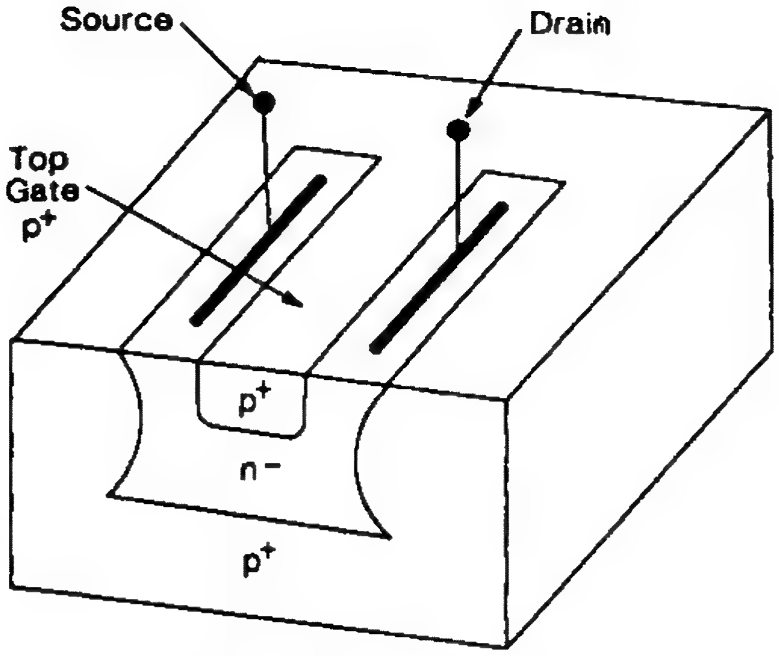


Figure 4.24 Cutaway view clearly shows that the gate totally surrounds the active area of the JFET.

Historically, some gate overhang was tolerated to ensure alignment, but this overhang contributes to C_{gd}.

Today, most MOSFETs that are fabricated use special techniques that eliminate overhand and with it, lower C_{gd}.

DMOSFET (Power)

Whereas with most FETs, the applied voltage affects (modulates) the depletion width, which, in turn, affects the interterminal capacitances, for the classic power DMOSFET (Figure 1.18), the drain-source voltage V_{DS} modulates the effective *plate area* of our capacitor.

We can visualize the effect by closely examining Figure 4.22. where we see that the epi-depletion thickness $W_{d(epi)}$, effectively alters the plate area beneath the gate oxide. As a result, C_{gs} does *not* vary according to the classic $1/(V_{DS})^{1/2}$, but in proportion to $1 - K(V_{DS})^{1/2}$.

A not-too-subtle effect occurs when the magnitude of V_{DS} drops *below* V_{GS} (a common occurrence when a transistor is used as a switch). The channel and the n-epi region beneath the gate oxide are flooded with carriers. If we now visualize Figure 4.22 with a substantially larger conduction area beneath the oxide, we will not be surprised at the substantially higher C_{gd}. Using our model—the 400 V, 1 Ω DMOSFET—note the

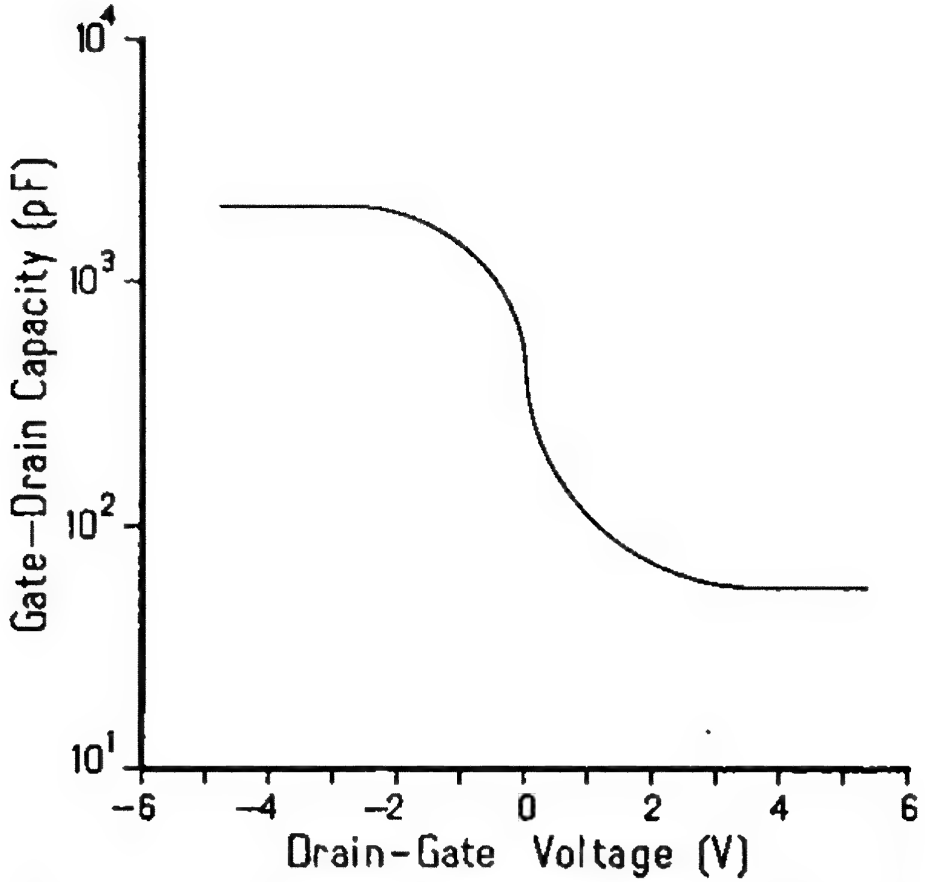


Figure 4.25 During the switching cycle of a power DMOSFET, once V_{GS} exceeds V_{SAT} (V_{DG} crosses zero), C_{gd} rises rapidly to extraordinary levels and is the major contributor to establishing the switching time specifications.

change in C_{gd} when V_{DS} drops *below* V_{GS} by comparing Figure 4.25 with Figure 4.18.

4.2.27 $t_{d(on)}$ *Turn-ON Delay Time*

For *any* FET, $t_{d(on)}$ denotes the inverval of time necessary for the gate drive to activate the FET. Regardless of FET type (JFET, MOSFET, SIT, IGBT), the mitigating parameters that ultimately control this characteristic are the *input capacitance* and the magnitude of gate control (whether $V_{GS(off)}$ for depletion-mode FETs or $V_{GS(th)}$ for enhancement-mode MOSFETs).

All FETs, like bipolar transistors, are *charge*-controlled devices. That is, a finite charge must be injected into, or out of, the gate to prompt the FET into action. Unlike the bipolar transistor, this charge does not need to be maintained; it must only charge or discharge the input capacitance to bring the gate voltage into compliance to attain the desired action.

We can express this charge control as follows:

$$i_{in} = \frac{dQ}{dt} \tag{4.21}$$

where i_{in} is the charging current required to bring the input capacitance into compliance. The current may be defined as follows:

$$i_{in} = C_{in} \frac{dV_{GS}}{dt} \tag{4.22}$$

and, in combining Eqs. 4.21 and 4.22, we find:

$$C_{in} = \frac{dQ}{dV_{GS}} \tag{4.23}$$

If we follow the gate-charge characteristics in Figure 4.26 (for this illustration our model is a 400 V, 1 Ω power DMOSFET) with the switching waveform shown earlier in Figure 3.2, we should achieve a reasonably clear appreciation of how switching times are affected by FET capacitances. Although these figures pertain to the power DMOSFET, the principles apply to *any* FET.

Initial turn-ON delay $t_{d(on)}$, begins with no charge, hence no gate voltage when the input pulse impinges on the gate terminal. As charge begins to build on the input capacitance C_{in}, we see the gate voltage V_{GS}, rise (region 1 in Figure 4.26). We may deduce C_{in} from the slope of V_{GS}, using Eq. 4.23.

4.2.28 t_r *Rise Time*

For *any* FET, t_r identifies the portion of time during which the gate has activated the FET to produce a dramatic change in drain voltage as witnessed in Figure 4.26 and compared with Figure 3.2.

Although we indeed see the expected dramatic change in V_{DS} (region 2 of Figure 4.26), we also observe a dramatic slowing of the gate voltage V_{GS}, ramp (and, according to Eq. 4.23, a dramatic increase in C_{in}) due to a phenomenon called *Miller effect*.

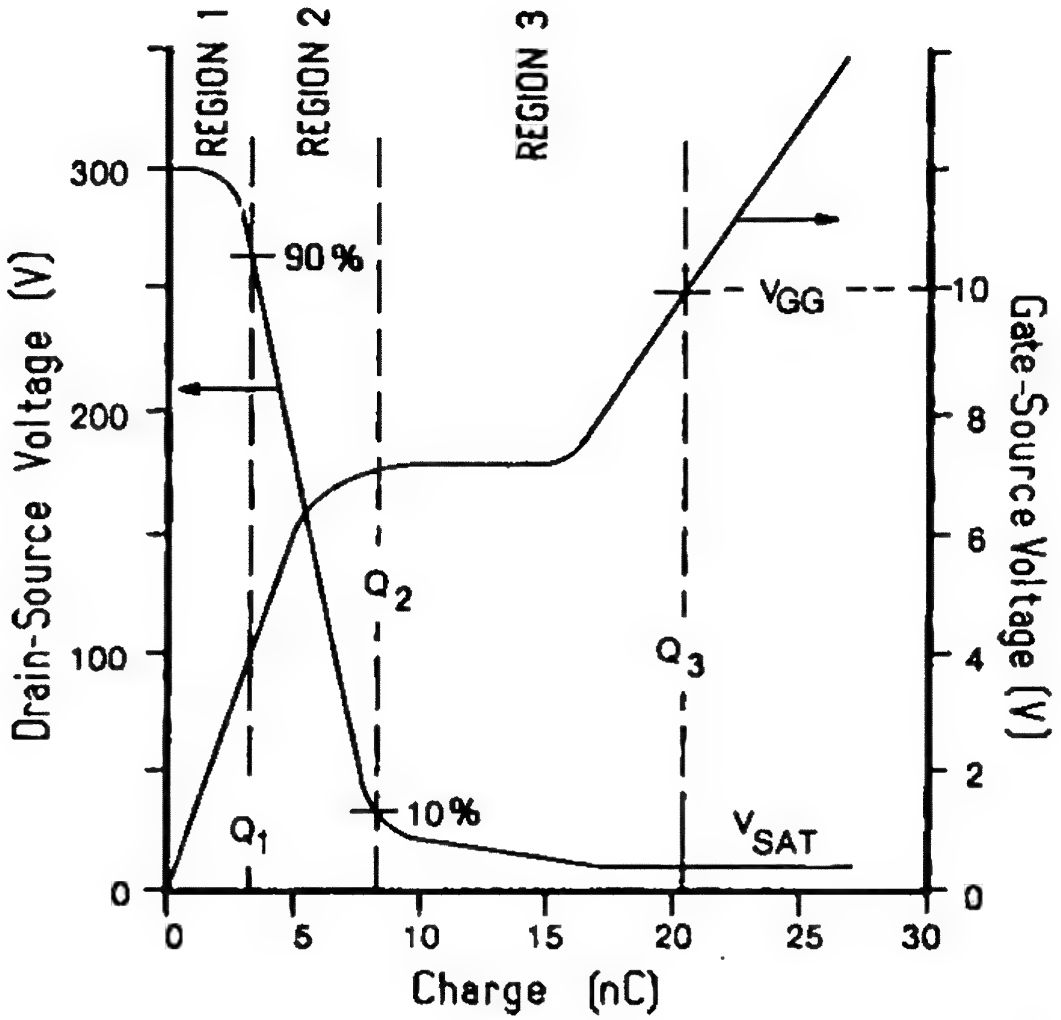


Figure 4.26 Typical charge curve of a power DMOSFET, showing the charge on the gate as well as the collapsing drain voltage during switching. Region 1 extends to threshold, region 2 covers the switching period (from 90% to 10% of the voltage waveform), and region 3 goes to full saturation. Note especially that V_{SAT} occurs at the point at which V_{GS} resumes its climb to V_{GG}. The slow settling to V_{SAT} (in region 3) is due to the rise of C_{gd} (Figure 4.25).

The Miller Effect

An amplifying element, whether bipolar transistor, FET, or vacuum tube, operating in—using FET terminology—the common-source configuration (source common to both input and output) has both an input and a feedback capacitance that, depending on the voltage gain of the stage μ, will merge to form an equivalent input capacitance, $C_{in(eq)}$:

$$C_{in(eq)} = C_{gs} + C_{gd}(1 - \mu) \quad (4.24)$$

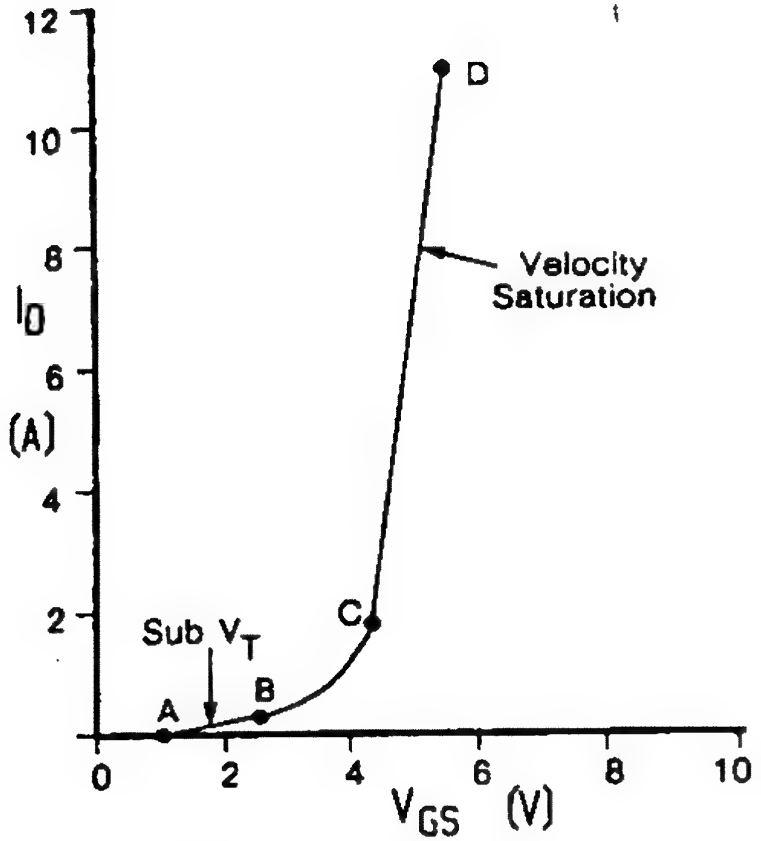


Figure 4.27 Transfer characteristics of the power DMOSFET showing the three principal regions: subthreshold (A—B), square-law (B—C), and velocity-saturated (C—D).

Since, from Eq. 4.14,

$$\mu = -g_{fs} R_d$$

we have:

$$C_{in(eq)} = C_{gs} + C_{gd}(1 + g_{fs}R_d) \qquad (4.25)$$

Remembering Eq. 4.7, g_{fs} is directly proportional to a change in drain current, dI_d. FETs, in general, exhibit a triple-state transfer characteristic as shown in Figure 4.27, where we witness a slow turn-ON. Consequently, we see in Figure 4.26, a gradual increase in C_{in}, shown by the flattening of the gate charge, as μ increases.

According to Eq. 4.7, when dI_D approaches zero (at current saturation), our voltage gain μ also decays to zero, at which instant the Miller effect vanishes and, as we see from Figure 4.26, the gate charge once more rises until V_{GG} (the original gate-drive voltage) is attained.

On the data sheets of some smaller FETs we often do not find either $t_{d(on)}$ or t_r; rather, we see the symbol $t_{(on)}$; which represents the *sum* of $t_{d(on)}$ and t_r.

4.2.29 $t_{d(off)}$ *Turn-OFF Delay Time*

For a FET, this delay time is not as serious a problem as it is for the typical bipolar transistor or IGBT. To ensure turn-OFF we need to *reverse* the charge on both the input and output capacitances. Whereas for turn-ON we might have raised the gate potential (as we did for the power DMOSFET in Figure 4.26 and for the JFET by bringing the bias V_{GG}, from beyond cutoff to $V_{GS} = 0$) and, likewise, dropped the drain voltage, which, in turn, would have discharged the output capacitance C_{oss}, now we must reverse the charge on C_{in} and charge C_{oss}. The interval of time we need to drop V_{GS} from our turn-ON potential of V_{GG} to the point at which turn-OFF begins is "dead" time. Truthfully, a form of *storage time*!

IGBT

The IGBT, however, like the bipolar transistor, suffers from storage time—a phenomenon whereby the minority carriers injected into the n-epi region from the p-substrate (collector) (Figure 1.20) require a finite time to recombine before the device truly turns OFF.

4.2.30 t_f *Fall Time*

Like rise time, fall time is seriously affected by the Miller effect. As V_{GS} enters into the square-law region of the transfer characteristic ("C" in Figure 4.27), the voltage gain μ drops, and we see a corresponding de-emphasis of the Miller effect (Figure 4.28).

Reviewing the switching time specifications, we must not forget that the FET parameters of V_T (for enhancement-mode devices) or $V_{GS(off)}$ (for depletion-mode devices) play a critical role as we juggle our specifications. Note, for example, that as we lower V_T, we shorten $t_{d(on)}$ but lengthen $t_{d(off)}$. Likewise there are tradeoffs with the depletion-mode FETs as we try matching our gate drive to $V_{GS(off)}$.

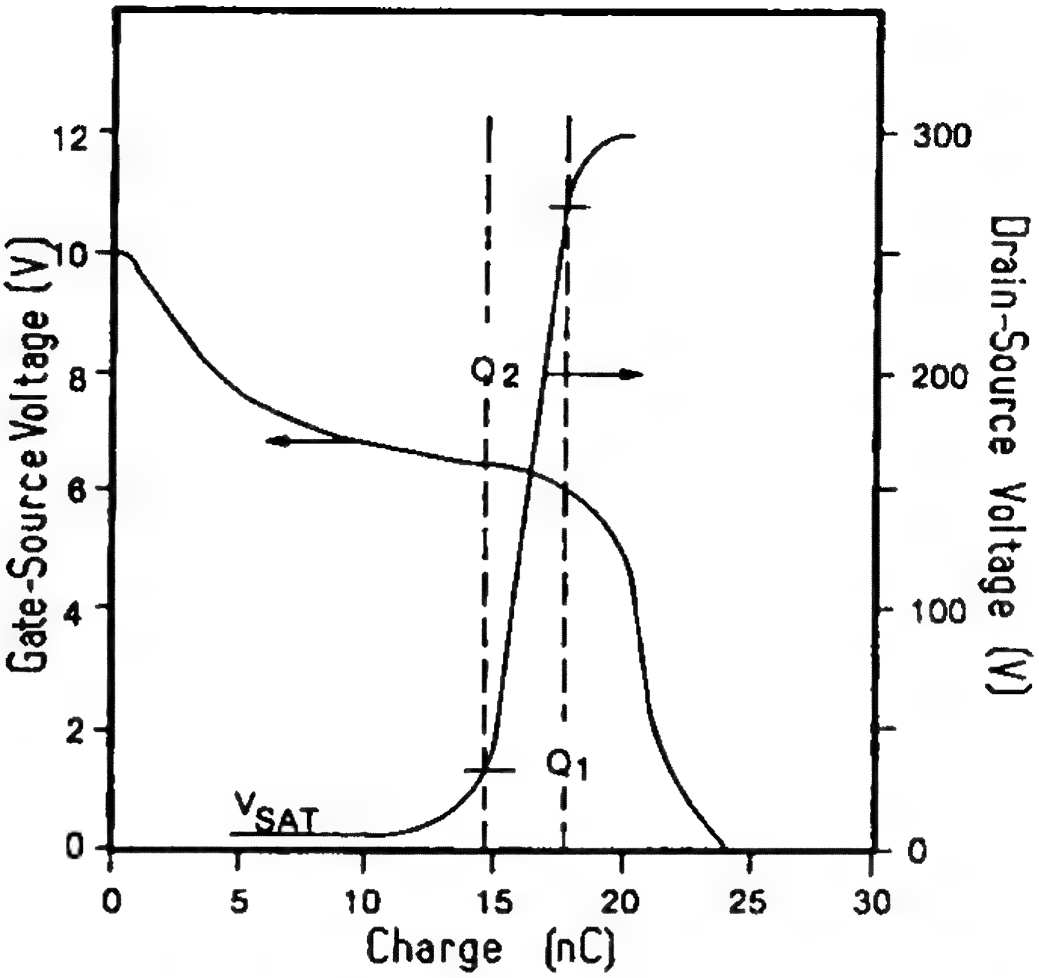


Figure 4.28 Turn-OFF charge characteristics of a power DMOSFET. Note that the Miller effect is less prominent than at turn-ON (Figure 4.26).

Because of the plethora of FETs and FET specifications, it is often difficult to select the fastest FET. The simplest and most accurate method would be to compare the gate-charge waveforms.

We saw on the data sheets of some small FETs that symbols for $t_{d(off)}$ and t_f have been replaced by their *sum*: $t_{(off)}$.

4.2.31 t_{rr} *Reverse Recovery Time*

This parameter of the power DMOSFET body-drain diode is best understood by reexamining Figure 3.3. If we consider a diode in forward conduction, the depletion fields are fully collapsed and the carriers are freely flowing across the pn junction. If we abruptly reverse the carrier flow, the diode will not abruptly cease conducting because it takes a finite time to reestablish the depletion fields and to sweep the excess carriers out of the region. The time is called *reverse recovery time*; the excess

carriers are called *minority carriers* and constitute an unwanted charge Q_{rr} (also identified as Q_s).

In the design of power transistors, including FETs and IGBTs, we try to shorten both t_{rr} and the number of minority carriers. If we compare t_{rr} with the switching times associated with most power DMOSFETs, we see that the former is quite slow.

The speed of this diode is a function of the area labeled Q_s—stored charge (Figure 3.3). On a data sheet we find, not Q_s, but t_{rr}—the time elapsed between the current's passing of the zero crossing and returning to with 10% of its pink reverse value.

This elapsed time depends on many measurement variables, which we must identify as we begin comparing one manufacturer's product against another. Among the variables we have:

1. The initial forward current, I_D
2. The rate of fall of current, $-di/dt$
3. The chip temperature, T_J

Besides Q_s we need to be aware of the *shape* of the recovering-current waveform (the positive-going portion of the waveform in Figure 3.3, labeled $+dI_R/dt$). If it exhibits a fast rise, we may experience a "snap," and with it, a sharp voltage spike across any inductive load we may be controlling with the power DMOSFET. A sharp snap conceivably could generate a voltage transient that exceeds the $V_{(BR)DSS}$ of the FET ($E = L\ di/dt$)! This is more fully explained in Chapter 5.

Among the design options opened to us to reduce t_{rr} are specialized doping and epitaxial growth, irradiation, and contouring of the diffusions.

4.2.32 Q *Charge*

Charge is an important parameter when we consider the switching speed as well as the maximum operating frequency of the FET. All FETs (and all bipolar transistors) are charged-controlled devices. If we seek a high-current (mobile-charge) switching FET, we discover that we need a proportionally higher charge to excite the FET. Likewise if we wish to switch more swiftly, we must move the charge more quickly. It is how we move the charge that determines how we use the FET. In driving our FET, as we add charge, Q^+, to the gate electrode;

across the dielectric we develop an equal charge, Q^- (see Figure 1.7). Our so-called drain current I_D, represents this charge, albeit as a continually moving charge.

Interestingly, charge is independent of temperature, which is one reason why we find the capacitive elements of a FET unaffected by changes in temperature

4.2.33 $Q_{g(th)}$ *Gate Threshold Charge*

The amount of charge that we must supply to reach threshold is represented by $Q_{g(th)}$.

4.2.34 $Q_{g(on)}$ *Gate Turn-ON Charge*

The charge required to reach the specified V_{GS} for $r_{DS(on)}$ measurement is shown as $Q_{g(on)}$.

4.2.35 $Q_{gm(on)}$ *Maximum Gate Turn-ON Charge*

The charge necessary to reach the maximum rated V_{GS}, symbolized as $Q_{gm(on)}$ is superfluous for most applications.

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5

Characterization, Part II

Parameter Action and Reaction

5.1 Introduction

In Chapter 4 we discussed how each parameter is achieved; now we learn how the parameters affect performance and how they interact one with another.

Again, the phenomenological approach is taken, using, only a few equations, as in Chapter 4. Equations can express concepts that might otherwise be lost in words if only word pictures are used.

Truthfully, parameters do not *affect* performance; they *define* performance. Nonetheless, in this chapter we take a critical look at parameters as if they *did* affect performance. In Chapter 7 we give ample space to the interpretation of desired (and *hoped for*) performance.

Indeed, parameters do interact; in fact, their interaction often become the Achilles' heel of the design engineer, who must compromise design objectives to achieve a workable solution. As we examine the FET parameters, it would be unforgivable not to also examine this interaction.

5.2 How Parameters Affect Performance

As Chapters 3 and 4, we take each parameter in turn, and if the parameter behaves differently for different FETs, we examine its performance for each type of FET.

5.2.1 $V_{(BR)DSS}$ *Breakdown Voltage, Drain to Source*

The parameter quite obviously identifies the maximum allowable voltage that can appear across our device, therefore defining our absolute maximum operating voltage. In practice we would not operate a device at this specified limit. On earlier data sheets the symbol was identified as BV_{DSS}.

There are subtle (and not so subtle) reasons for operating well below the rated breakdown voltage, which are addressed in subsequent chapters.

FETs (Small Signal)

Remembering how we interpret this symbol, we recognize that the gate is tied to the source, making $V_{(BR)DSS}$ nearly (but not quite) identical to BV_{GSS}. The small-signal JFET seldom is specified using this symbol simply because to do so would offer no guarantee that source and drain could be interchanged. The $V_{(BR)DSS}$ (for JFETs, more frequently identified as BV_{DSS}) offers no guarantee of *source*-gate breakdown, only drain-gate breakdown.

However, for that special case of asymmetrical JFETs, such as the 2SK19 and 2SK152 (and others), this parameter has special significance in our understanding of the breakdown characteristics, since gate-source breakdown is much less than gate-drain.

MOSFET (Small Signal, Depletion Mode)

Unlike the small-signal JFET, $V_{(BR)DSS}$ for the depletion-mode MOSFET also defines breakdown across the gate oxide to the drain diffusion. Since the test conditions imposed for this measurement require that the gate bias keep the MOSFET in the OFF condition (a fully depleted channel), we discover that our parameter, $V_{(BR)DSS}$, defines the drain-*gate* breakdown.

There are, however, other mechanisms of breakdown involved in the parameter $V_{(BR)DSS}$. If, for example, we bias the MOSFET into conduction, we see the expected output characteristic that, if extended to breakdown, identifies a subtle but certain relationship with V_{GS}, as shown in Figure 5.1. This phenomenon of *channel* breakdown is identified by the initial gradual increase in drain current, becoming quite abrupt as the drain voltage increases.

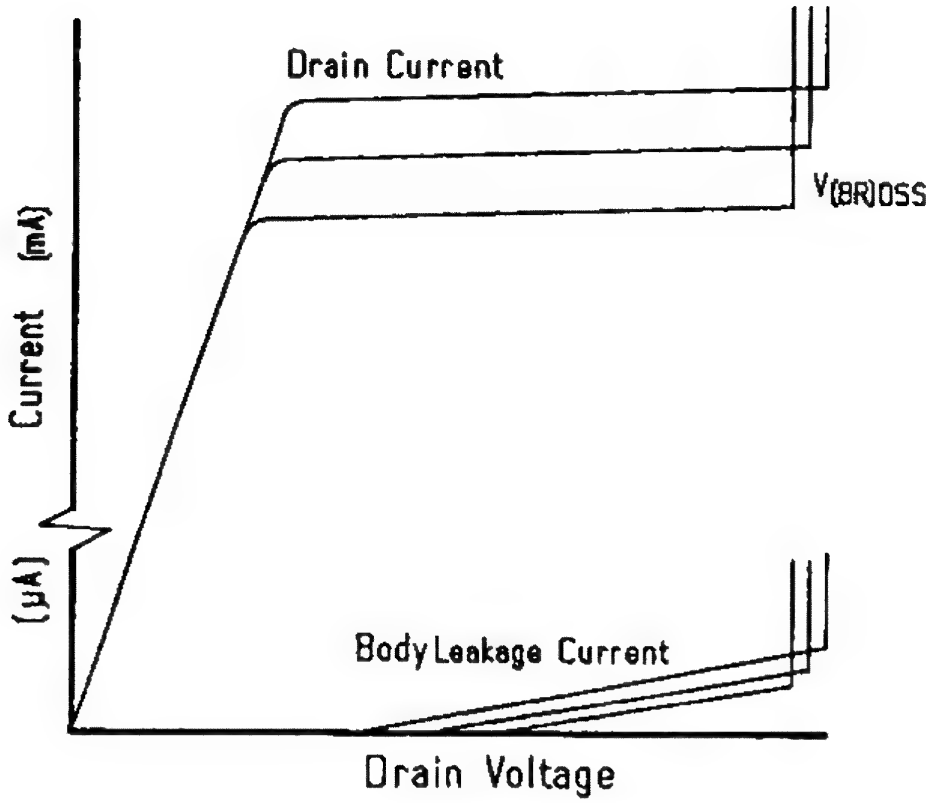

Figure 5.1 Output characteristics of a small-signal MOSFET showing the effect of gate bias on breakdown as well as the body (substrate)-drain leakage current. Note that the output characteristics are at least an order of magnitude larger than the substrate leakage currents.

This gradual increase in drain current results from at least two causes. Since the channel is enhanced, we may attribute the majority of this increase in current to channel breakdown; additionally, we find carrier *injection* into the substrate from the drain diode formed by the drain diffusion and substrate. In Figure 5.1 we see a gradual increase in substrate current that becomes increasingly sharp as we approach $V_{(BR)DSS}$.

With the MOSFET biased OFF ($V_{GS} > V_{GS(off)}$), we appear to identify two mechanisms that contribute to breakdown: the drain-to-gate breakdown, which also is dependent on V_{GS} and the drain-to-substrate breakdown, which is not specifically identified as $V_{(BR)DSS}$. The latter is related to the p-n diode that exists in the MOSFET (see Figure 1.8). It is interesting to note that the former is influenced by V_{GS}, as we saw in Figure 5.1.

Since V_{GS} plays a role in establishing the breakdown voltage of the MOSFET, we should also expect that a relationship exists between $V_{(BR)DSS}$ and $V_{GS(off)}$.

It is reasonable to expect that a thicker gate oxide will raise the breakdown voltage existing between drain and gate. In

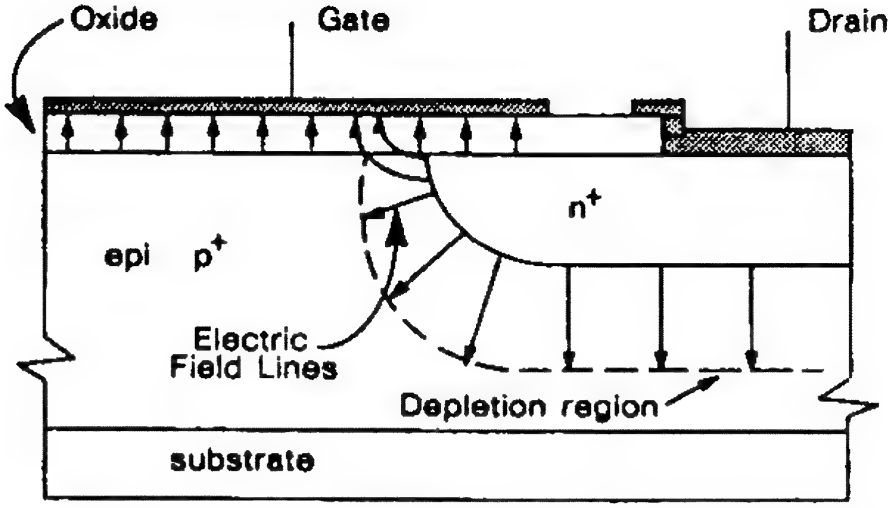

Figure 5.2 The drain portion of an n-channel MOSFET showing the approximate form of the electric field lines under cutoff conditions. (From Richard S. C. Cobbold, *Theory and Applications of Field-Effect Transistors*, copyright © 1971, John Wiley & Sons. Reprinted by permission of John Wiley & Sons, Inc.)

practice we can expect to withstand about 6×10^6 V/cm separation. If we increase the thickness, we discover that along with increasing $V_{(BR)DSS}$ we also have increased $V_{GS(off)}$. That is, it now takes a greater potential to effect cutoff. Additionally, as we thicken the gate oxide we reduce C_{gs} as well as C_{gd}, but transconductance, g_{fs}, suffers, as we saw from Eq. 4.10.

MOSFET (Small Signal, Enhancement Mode)

From an examination of Figure 1.8, it is reasonably clear that we have, as with the depletion-mode MOSFET, two areas in which breakdown can occur: at the drain-gate oxide, and at the pn (diode) interface formed by drain diffusion into the substrate. For this type of MOSFET, we find the breakdown phenomenon to be sensitive to the gate potential V_{GS}. This relationship is believed to be due to the influence of the gate potential on the drain-substrate depletion region, shown in Figure 5.2, as well as, of course, to the close proximity of the gate to the drain.

SIT

Because of the unusual cross-section of the static-induction transistor, the parameter $V_{(BR)DSS}$, does not specifically apply.

Rather, a parameter based on drain-*gate* breakdown is more appropriate (yet *not* BV_{GSS}), which we might lable BV_{DGO}—gate-drain with source not connected. For this device, breakdown is determined from the electric field distribution, which, in turn, is more a function of the depletion region formed between the gate and the drain, as well as the carrier mobility, both of which depend on epi resistivity.

To alleviate premature breakdown, the SIT, like most high-voltage transistors, relies on the judicious placement of field control elements (see Section 4.2.1).

Several conflicts become obvious as we work to raise the breakdown voltage characteristics. Any lengthening of the gate-to-drain distance will tend to modify the output characteristics, and we see the SIT behaving less like a triode and trending more toward the classic JFET pentode characteristic, as in Figure 5.3. Yet, as the gate-drain distance is adjusted for optimum breakdown, gate control changes, resulting in changes in $V_{GS(off)}$, the amplification factor μ (see Eq. 4.11), and transconductance (see Eq. 4.14).

Quite unlike the JFET, the source-gate breakdown is generally considerably less than the drain-gate breakdown.

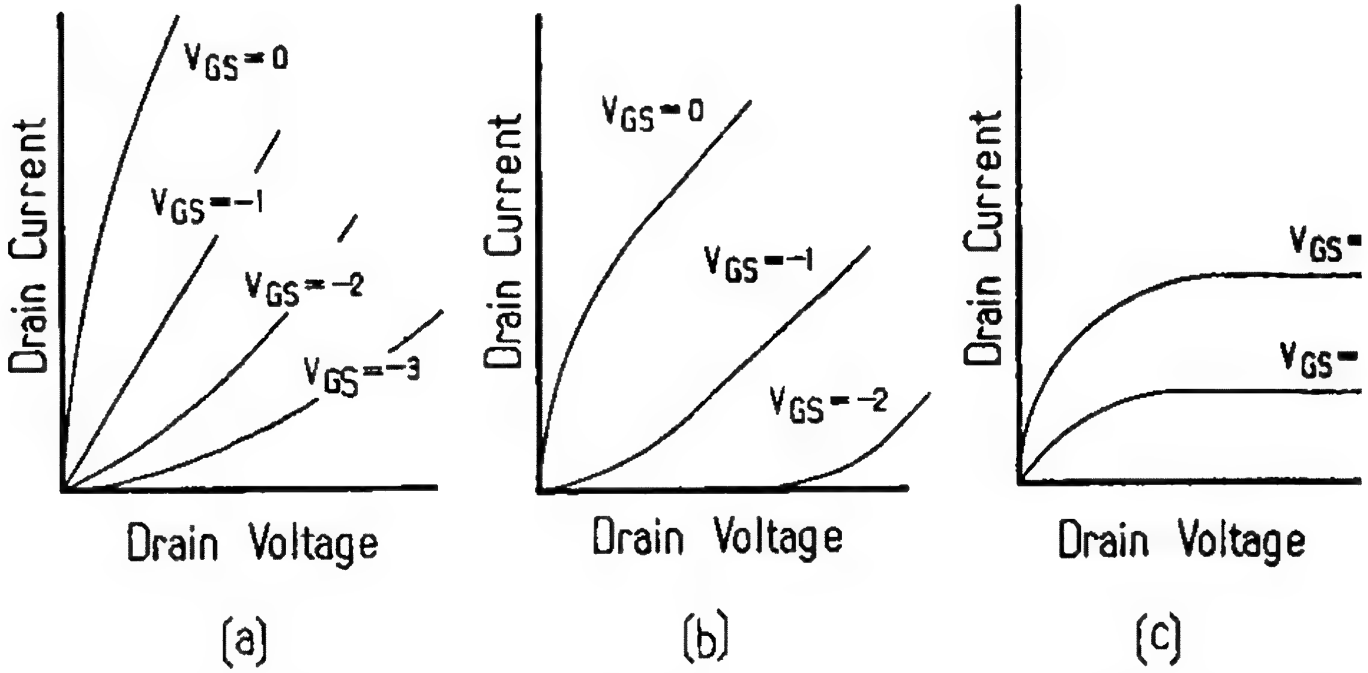

Figure 5.3 Output characteristics of the static-induction transistor showing the effect of gate length (micrometers): (a) short gate, 1μ, (b) 2μ, and (c) 4μ. (From Yamaguchi and Kodera, "Optimum Design of Triode-Like JFETs by Two-Dimensional Computer Simulation," copyright © 1977, *IEEE Transactions on Electron Devices* ED-24, 1061-69 (August 1977). Used with permission.)

DMOSFET

As we have seen in earlier chapters, the breakdown voltage of a power DMOSFET is not always a reflection of the channel parameters but of the epi resistivity (see Eq. 4.5 and following discussion), which, in turn, affects the ON resistance. What does affect the breakdown characteristics is the pn (channel-epi) junction as well as the field control elements.

Avalanche breakdown, $V_{(BR)DSS}$, implies a sudden multiplication of carriers, leading to such heavy currents that we have a disastrous thermal effect resulting in burnout.

Since breakdown and ON resistance are intertwined (Eq. 4.5), so also are the parameters that depend on $r_{DS(on)}$: I_D (Eq. 3.1), $I_{D(on)}$ (Section 4.2.10), I_{DM} (Section 4.12), $V_{DS(on)}$ (Section 4.2.3), and g_{fs}. As $V_{(BR)DSS}$ rises, we see the currents decrease, the saturation voltage rise, and the transconductance fall.

IGBT

The breakdown characteristics of the insulated-gate bipolar transistor are closely analogous to that of the power bipolar transistor with an *open* base (for the n-channel IGBT, we refer to an open-base pnp structure, see Figure 1.20). Since, like the bipolar transistor, breakdown is first controlled by the terminations and second by the epi doping levels, we can anticipate some interdependence between BV_{CEO} and I_C.

5.2.2 $V_{(BR)GSS}$ *Breakdown Voltage, Gate to Source*

This parameter has particular meaning for the small-signal JFET simply because it defines not only the gate-source breakdown but drain-source breakdown as well. This because the drain and source are electrically bonded for the measurement.

Again, for those asymmetrical 2SK19 and 2SK152, mentioned earlier, this parameter holds little meaning aside from being known to be of a lower magnitude than $V_{(BR)DSS}$.

5.2.3 $V_{DS(on)}$ *ON State Drain-Source Voltage* (also known as V_{SAT} or $V_{DS(sat)}$)

This parameter, which applies principally to the characterization of power transistors, such as the power DMOSFET and the IGBT, is the product of drain current and ON resistance:

$$V_{DS(on)} = I_D R_{DS(on)} \tag{5.1}$$

Thus we immediately are able to recognize its relationship to both the drain current and the ON resistance. Not that this parameter affects those parameters; quite the contrary, we see $V_{DS(on)}$ affected by them.

Regardless of our choice of transistor, we desire a low $V_{DS(on)}$, if for no other reason than to conserve power. Equation 5.1 identifies the magnitude of voltage resulting from a finite ON resistance; Eq. 5.2 identifies the power lost:

$$P_D = I_D^2 R_{DS(on)} = V_{DS(on)} I_D \tag{5.2}$$

Unlike both the power bipolar (BJT) and the insulated-gate bipolar transistors, turn-OFF delay, $t_{d(off)}$, more commonly known as *storage time*, is little affected by $V_{DS(on)}$. What little effect we see focuses, in part, on the charge characteristics of the output capacitance. This value of capacitance is set by the ON voltage across the depletion region resident in the epi layer immediately beneath the body diffusion. As a result, a higher $V_{DS(on)}$ tends to offer a slightly *faster* turn-OFF!

During the turn-ON switching cycle, when the magnitude of V_{DS} drops below the magnitude of V_{GS} (eventually stopping at $V_{DS(on)}$), we discover a startling increase in the Miller capacitance (see Figure 5.4) that dramatically *slows* the time to achieve full saturation ($V_{DS(on)}$). This is quite noticeable when viewing the drain voltage versus gate charge switching curves shown in Figure 5.5.

5.2.4 $V_{GS(f)}$ *Gate-Source Forward Voltage*

This voltage applies only to gold-eutectic, die-attached JFETs that utilize the underside of the chip as a gate contact. As a result of either contamination or improper soldering temperatures,

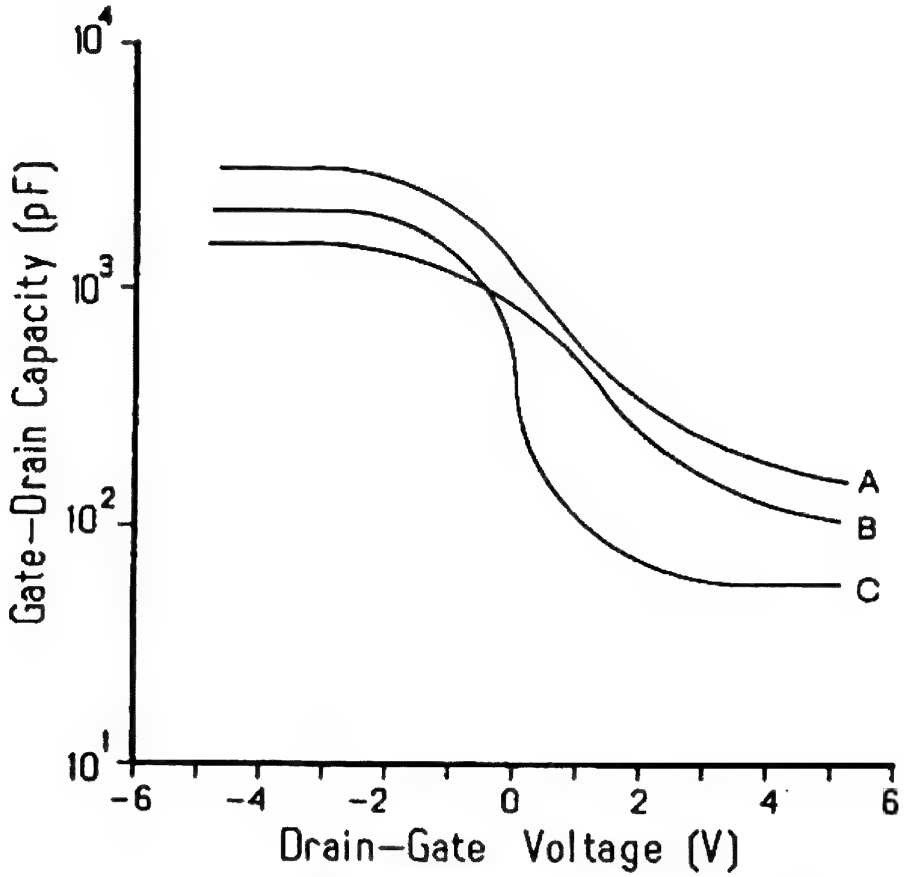

Figure 5.4 Effect of drain-gate voltage on the feedback capacitance C_{gd} during turn-ON of a power DMOSFET. When V_{DS} drops below V_{GS}, a sudden and dramatic increase in C_{gd} occurs due to the flooding of carriers immediately beneath the gate oxide.

the gold eutectic-to-silicon bond may revert into a low-grade (Au-Si) Schottky diode. When this occurs, we see severe performance degradation with respect to any gate-controlled parameter, such as transconductance (gain) or noise figure. There is little or no effect on operating gate current I_G.

5.2.5 $V_{GS(off)}$ *Gate-Source Cutoff Voltage*

This parameter applies to any depletion-mode FET or MOSFET. Although $V_{GS(off)}$ defines that gate voltage required to turn the FET OFF, it actually defines most of the critical electrical parameters of the JFET.

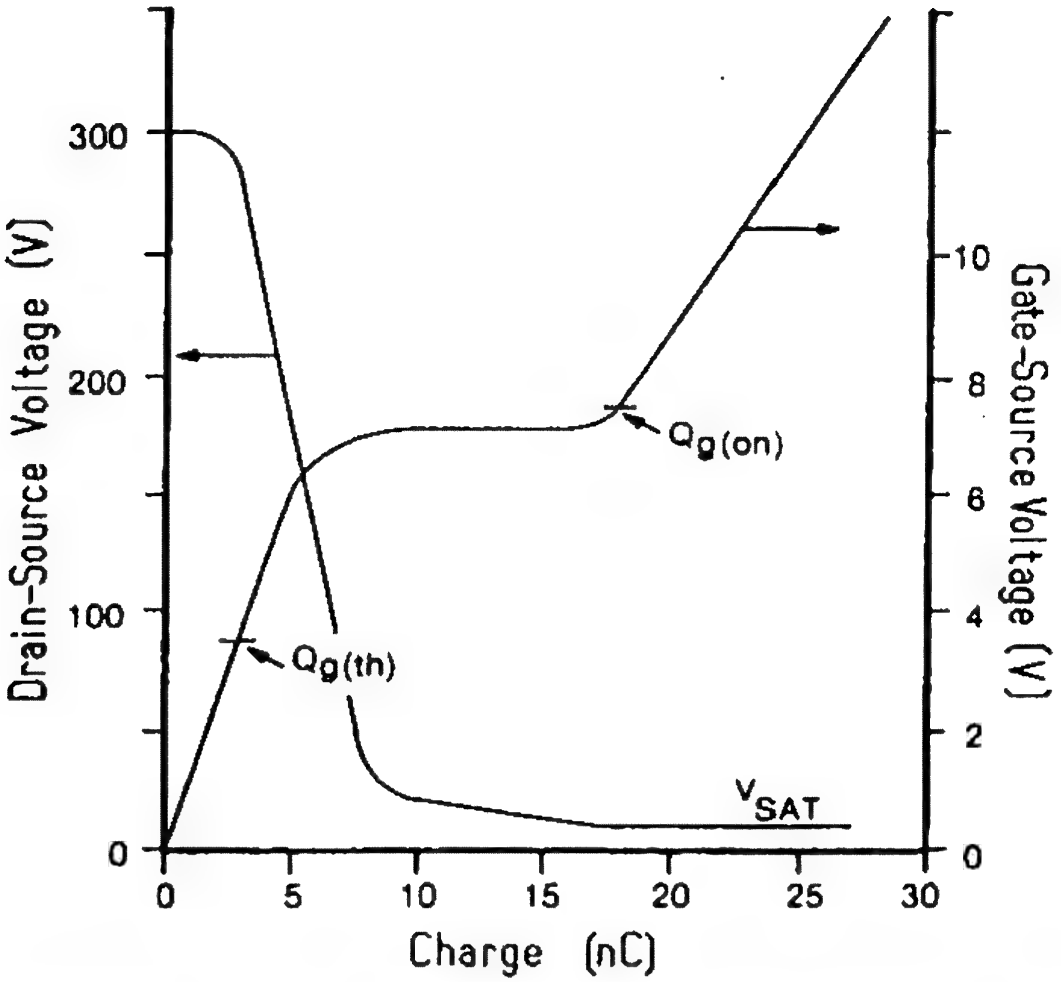

Figure 5.5 Turn-ON charge characteristics of the typical power DMOSFET. The extended flat region of the gate charge is cause by the sudden increase in C_{gd} shown in Figure 5.4.

JFET

Among the parameters affected directly by $V_{GS(off)}$ are I_{DSS}, $R_{DS(on)}$, and g_{fs}, as well as g_{os} and the variation of I_{DZ} (zero temperature coefficient drain current).

Shockley's equation (Eq. 2.2) forms the basis of this interdependency for the JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (5.3)$$

from which we can derive most, if not all of the equations that define JFET performance. Differentiating Eq. 5.3 with respect to V_{GS} provides us the equation for transconductance:

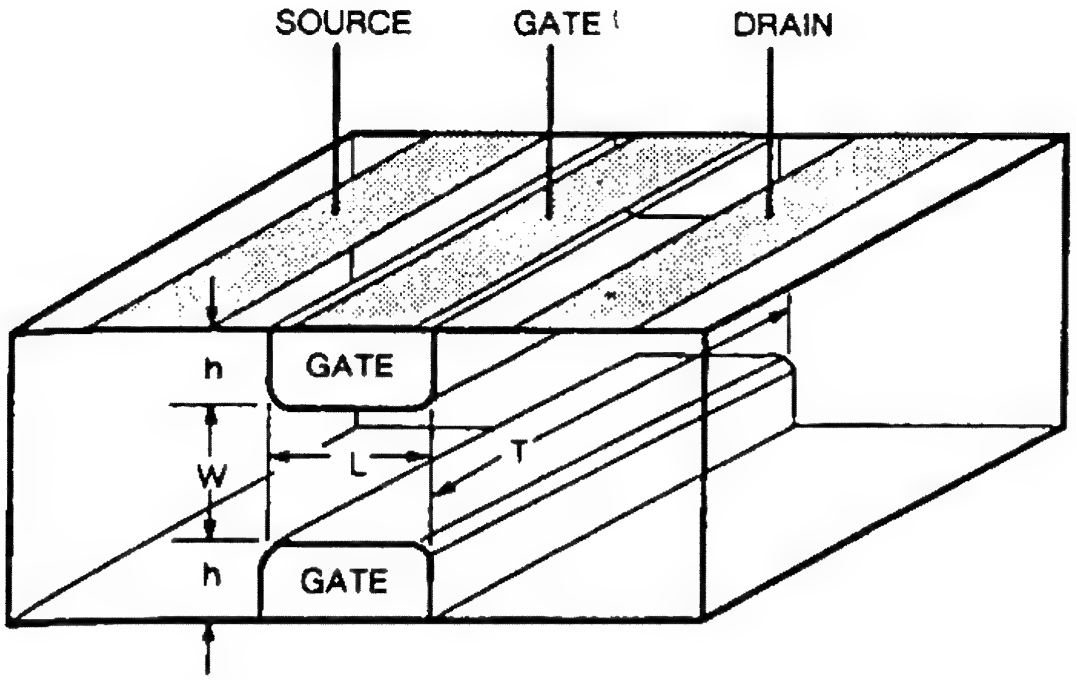

Figure 5.6 Cross-sectional view of the JFET showing the three critical channel dimensions that influence performance.

$$g_{fso} = K \frac{I_{DSS}}{V_{GS(off)}} \tag{5.4}$$

where K is generally presumed to be equal to 2, although in practice it may vary between 1.8 to 2.3 depending on the particular geometry.

The lateral (surface) dimensions of the JFET are established by the *photolithographic* process, but the cross-sectional dimensions, as shown in Figure 5.6, are established by *diffusion* processing. Such variables as temperature and doping concentrations will cause the p-doped gate to vary in depth (h) and width (L). These, in turn, vary the area of the JFET channel (WLT); which, in turn, affects performance. The relationships may be expressed by the following equations:

$$V_{GS(off)} - K_1 T^2 \tag{5.5}$$

$$I_{DSS} = K_2 T^3 \frac{W}{L} \tag{5.6}$$

We can merge Eqs. 5.5 and 5.6 into Eq. 5.4:

$$g_{fso} = K_3 T \frac{W}{L} \tag{5.7}$$

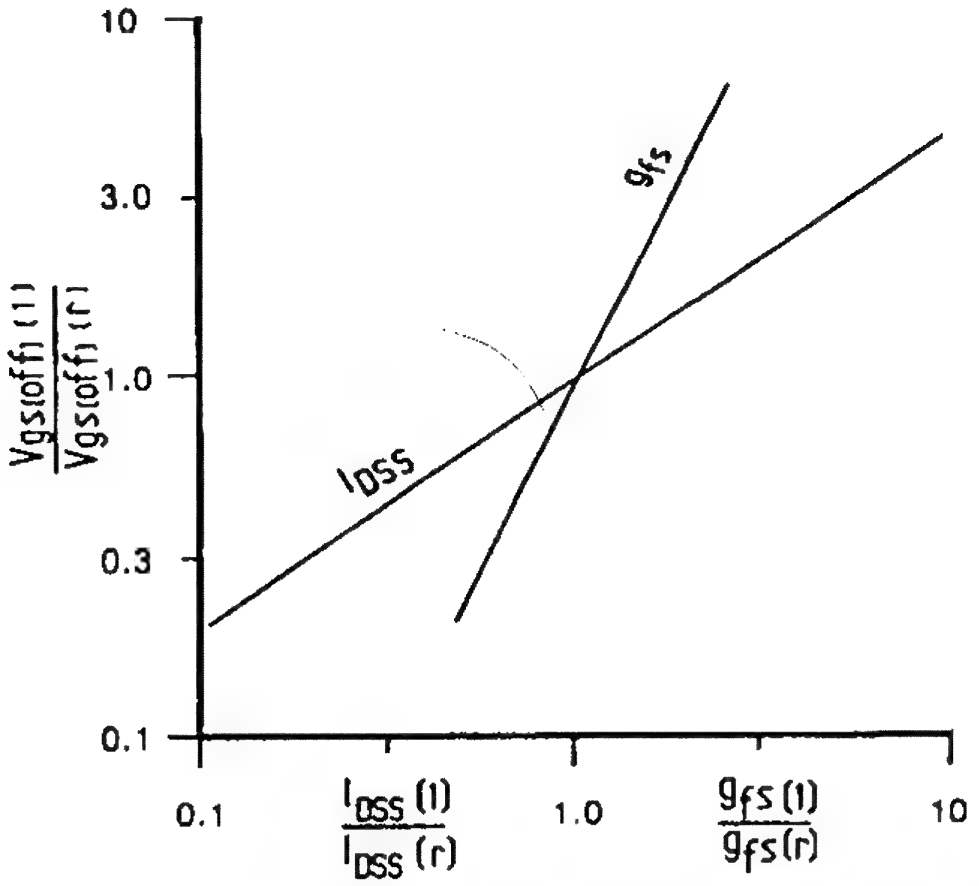

Figure 5.7 This universal scaling chart (for JFETs *only*) is applicable for any *one* geometry, of any *one* manufacturer, to obtain typical performance at other levels of gate-source cutoff voltage or saturation drain current.

Note that $V_{GS(off)}$ is proportional to the *square* of the channel thickness T, whereas I_{DSS} is proportional to the *cube* of channel thickness.

Throughout, K through K^3 simply reflects numerical constants. We can combine Eqs. 5.5 and 5.6, and Eqs. 5.6 with 5.7:

$$\frac{I_{DSS}(1)}{I_{DSS}(r)} = \left(\frac{V_{GS(off)}(1)}{V_{GS(off)}(r)}\right)^{3/2} \tag{5.8}$$

$$\frac{g_{fso}(1)}{g_{fso}(r)} = \left(\frac{I_{DSS}(1)}{I_{DSS}(r)}\right)^{2/5} \tag{5.9}$$

which, when plotted, as provided in Figure 5.7, allows us to scale the operating parameters of any JFET geometry.

Not only does $V_{GS(off)}$ directly affect I_{DSS} and g_{fs}, it also affects $R_{DS(on)}$:

$$R_{DS(on)} \cong \frac{(V_{GS(off)})^2}{K\ I_{DSS}(V_{GS(off)} - V_{GS})} \tag{5.10}$$

Since $R_{DS(on)}$ is tested at $V_{GS} = 0$, Eq. 5.10 simplifies to:

$$R_{DS(on)} \cong \frac{V_{GS(off)}}{K\ I_{DSS}} \tag{5.11}$$

Despite the simplification, when exercising this equation to derive the ON resistance, we must ascertain that our value of I_{DSS} is truly that zero-biased drain current when $V_{DS} = V_p$ (see Eq. 2.1). Invariably, when we seek to pull these parameters from a data sheet we discover that for $R_{DS(on)}$, V_{DS} is kept at a very low value, say 0.1 V (always considerably less than V_p), but for I_{DSS}, V_{DS} is set generally higher than 10 V, many volts beyond V_p. Consequently, to simply use these equations (i.e., Eqs. 5.10 and 5.11) to confirm the recorded parameters will tend to be a frustrating experience.

MOSFET (Depletion Mode)

By now we recognize that the MOSFET has an insulated gate, not a diffused gate like the JFET. Therefore, we might not expect $V_{GS(off)}$ to have quite the same influence over the MOSFET parameters as it does with the JFET.

Shockley's equation (Eq. 2.2, repeated in Eq. 5.3) does not apply to the performance of the depletion-mode MOSFET! Consequently, the derivations we examined for the JFET do not apply. For the saturated drain current I_{DSS}, the equation becomes unwieldy, but for an approximation, we may begin by using:

$$I_D \cong \frac{K}{2(V_{GS} - V_{GS(off)})^2} \tag{5.12}$$

where, in this case, K identifies a complex constant based on the MOSFET geometry.

Transconductance, g_{fs}, is, as before, the derivative of Eq. 5.12,

$$g_{fs} \cong K(V_{GS} - V_{GS(off)}) \tag{5.13}$$

For both Eqs. 5.12 and 5.13, V_{GS} exceeds $V_{GS(off)}$ and V_{DS} exceeds $|(V_{GS} - V_{GS(off)})|$. Ideally, once $V_{DS} = |(V_{GS} - V_{GS(off)})|$, both I_D (of Eq. 5.12) and g_{fs} (of Eq. 5.13) *saturate*. Below saturation, I_D and g_{fs} are functions of *both* V_{GS} and V_{DS}:

$$I_D \cong K\left[(V_{GS} - V_{GS(off)}) - \left(\frac{V_{DS}^2}{2}\right)\right]$$

$$\text{and} \quad g_{fs} = \frac{dI_D}{dV_{GS}} \tag{5.14}$$

Whether JFET or MOSFET, $V_{GS(off)}$ is temperature dependent. For the JFET we observe a dependence equal to the usual pn-junction dependency, averaging -2.22 mV/°C. In other words, as the operating temperature rises for an n-channel (or p-channel!) JFET, our cutoff voltage becomes increasingly more negative.

5.2.6 $V_{GS(th)}$ *Threshold Voltage*

The threshold voltage applies to any enhancement-mode MOSFET, and, like $V_{GS(off)}$ for the depletion-mode MOSFET, this parameter also affects several other parameters. Following Eqs. 5.12 and 5.13, we have:

$$I_D \cong \frac{K}{2(V_{GS} - V_{GS(th)})^2} \tag{5.15}$$

$$g_{fs} \cong K(V_{GS} - V_{GS(th)}) \tag{5.16}$$

Again we assume that V_{GS} exceeds $V_{GS(th)}$ and V_{DS} exceeds $(V_{GS} - V_{GS(th)})$. As with the depletion-mode FET, when we operate below saturation, both I_D and g_{fs} are influenced by V_{DS}, as Eq. 5.14 identifies (for the enhancement-mode MOSFET, $V_{GS(th)}$ replaces $V_{GS(off)}$).

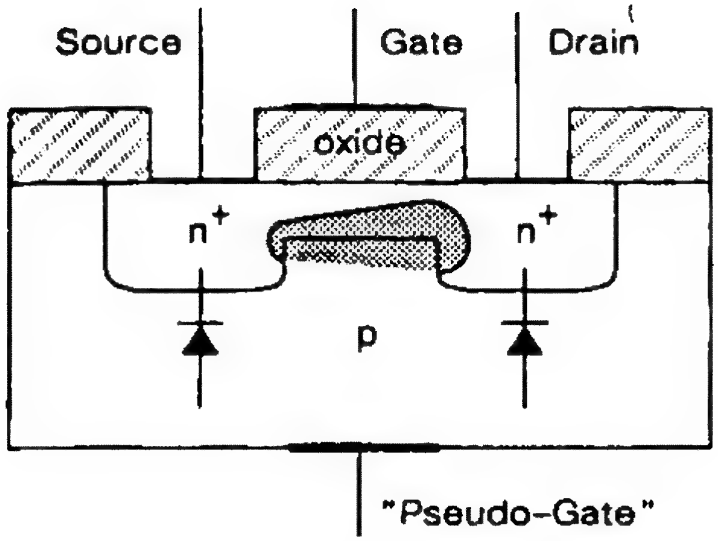

Figure 5.8 Substrate bias may affect threshold due to the pseudo-gate effect.

A disquieting influence on $V_{GS(th)}$ may be the substrate bias (always maintained in the reverse bias mode). As this bias is increased, a JFET-like depletion region may adversely affect the ON state, appearing to force the threshold up and making a higher gate bias necessary to maintain drain-current conduction. The effect is depicted in Figure 5.8.

The temperature effects on threshold are much the same as for $V_{GS(off)}$ for the JFET. An approximation for this dependency is:

$$\frac{d|V_{GS}|}{dT} = n - 2.5[|V_{GS} - V_{GS(th)}|] \text{ mV/°C} \qquad (5.17)$$

where n lies between 2 and 6, being dependent on the substrate doping. The term $|V_{GS} - V_{GS(th)}|$ suggests that the dependency is a function of I_D; consequently, we find that the MOSFET can exhibit either positive, negative, or zero temperature coefficeints depending on its drain current! This is true for MOSFETs in either mode (depletion or enhancement).

5.2.7 V_p *Pinch-Off Voltage*

The pinch-off voltage is often confused with $V_{GS(off)}$, and for years these two terms were frequently used interchangeably despite the opposing polarities. As with $V_{GS(off)}$, both I_{DSS} and $R_{DS(on)}$ are functions of V_p. However, whenever we see

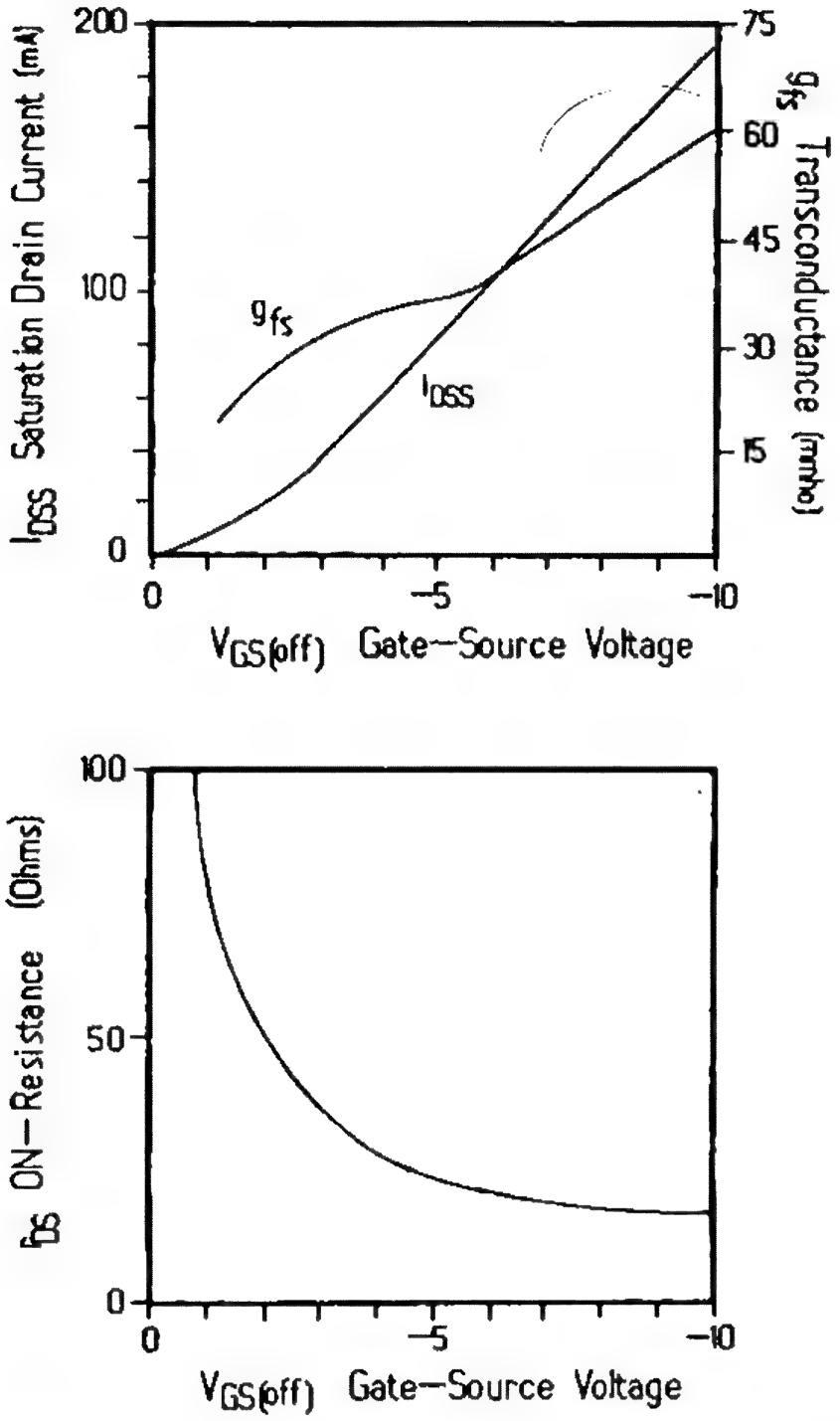

Figure 5.9 In manufacture, $V_{GS(off)}$ is determined by the depth of the gate diffusion. By measuring this parameter, we can closely estimate I_{DSS} and g_{fs} *for a particular geometry.*

convenient curves depicting this relationship. as in Figure 5.9, we are cautioned to remember that the test conditions for these parameters may make calculation difficult (see Eq. 5.11 and accompanying text).

5.2.8 $I_{A(R)}$ *Avalanche Current*

This term confirms ruggedness among power DMOSFETs of similar or identical description, generally when comparing vendors. Although seemingly a simple test, the results are depend on several variables, such as the size (and Q) of the unclamped inductor, the speed at which the power DMOSFET is switched OFF, and the supply voltage.

The test closely resembles the mode 3 dV/dt test. Although the *means* of induced failure may differ, the physics of failure appears the same. Diode current I_S, flowing into the base dopant (see Figure 4.6b) develops a potential across the parasitic base resistance that, in turn, triggers the parasitic bipolar ON. With the combination of drain voltage and "drain" (diode) current, hot-spotting results, lowering the turn-ON potential of the parasitic bipolar device. A thermal regeneration (mesoplasma formation) quickly occurs leading to runaway—and irreversible failure.

5.2.9 I_D *Drain Current*

Perhaps more than any other single parameter, I_D directly affects the performance of FETs in many ways.

JFET

Establishing a drain current establishes the gain, or transconductance, g_{fs}. If we opt for fixed-current bias (constant current), the g_{fs} of a particular type will vary from JFET to JFET and with temperature.

The output conductance is affected by I_D. As we bias our drain current further removed from I_{DSS} (closer to cutoff), we discover a progressive lowering of g_{os}:

$$\frac{I_D}{I_{DSS}} = \frac{g_{os}}{g'_{os}} \tag{5.18}$$

where g'_{os} is that value of output conductance at I_{DSS}.

In Chapter 4 we discovered the effect I_D has on gate current, I_G, in small-signal JFETs (see Figure 4.8).

Additionally, I_D is important in defining the drift specifications of dual JFETs. Zero-drift dual JFETs may be derived mathematically:

$$I_{DZ} = I_{DSS}\left(\frac{0.63}{V_{GS(off)}}\right)^2 \tag{5.19}$$

where I_{DZ} is the zero-drift drain current.

Differentiating Eq. 5.19 with respect to I_D, we produce a value, K, that identifies the drift per unit change of I_D:

$$K = \frac{dV_{GS(drift)}}{dI_D} = \frac{-1 \times 10^{-3}}{(I_D/I_{DZ})^{1/2}} \text{ V/°C} \tag{5.20}$$

Since, as we see from Eq. 5.20, V_{GS} drift depends on I_D, the *differential* drift d may be greatly reduced by unbalancing the drain current between the two sides of the dual by an amount, dI_D:

$$dI_D = \frac{d}{K} \tag{5.21}$$

where K is determined from Eq. 5.20.

DMOS (Small Signal)

An interesting phenomenon not immediately apparent is that the p-substrate (of n-channel DMOS) acts as a pseudo-gate to the enhanced channel when the FET is ON. As the drain current/drain voltage rises, we again see the effect of "operating gate current," albeit it is, in reality, a substrate current!

DMOSFET (Power)

The parameter I_D involves the power dissipation of the package, the ON resistance, and the transconductance g_{fs}, of the transistor.

On the surface, it is this parameter that attracts the attention of potential users of power transistors, for by it, in conjunction with the breakdown characteristics, does one often make a selection.

We cannot overemphasize the importance of being familiar with the SOA (safe operating area) curves that usually accompany a data sheet before relying on this parameter during the selection process. We cover this, and other precautions relative to I_D in Chapter 6.

5.2.10 $I_{D(on)}$ *ON State Drain Current*

Coupled with the test voltage used in its characterization (usually twice $V_{DS(on)}$), this parameter identifies the ON resistance $R_{DS(on)}$, of the power DMOSFET. We need to question why, for many power DMOSFETs, the parameter $R_{DS(on)}$ is not always characterized at $I_{D(on)}$. When we study I_{DM}, we will see how drain current affects $R_{DS(on)}$ and $V_{DS(on)}$.

When a power DMOSFET is used as a switch, the major power loss is *conduction* loss, of which $I_{D(on)}$ and $R_{DS(on)}$ are the fundamental contributors (I^2R).

Additionally, when we switch power DMOSFETs we discover that the Miller effect is closely associated with $I_{D(on)}$; the higher the current, the longer it takes for $V_{DS(on)}$ to be reached. This phenomenon becomes increasingly clear as we restudy Figure 4.25. Transconductance g_{fs}, is also affected by $I_{D(on)}$. The higher the current, the higher the transconductance, and the greater the Miller effect.

5.2.11 $I_{D(off)}$ *Drain Cutoff Current*

This parameter specifically addresses JFETs used as switches. Since it is a leakage current, the larger the chip, the greater the value of $I_{D(off)}$ and, coincidentally, because of the larger chip, the lower the value of ON resistance, $R_{DS(on)}$.

In the unlikely situation that $I_{D(off)}$ were used to define $V_{GS(off)}$, the parameter would identify that voltage at which a set *pinch-off* current, ($I_{D(off)}$), was achieved. It is a more likely occurrence that this parameter would be offered at a gate bias that lies beyond cutoff ($V_{GS} > |V_{GS(off)}|$), thereby providing a value of $I_{D(off)}$ always less than the cutoff current at $V_{GS(off)}$.

5.2.12 I_{DM} *Pulsed Drain Current*

Generally the parameter I_{DM} is found only in the absolute maximum ratings column of power DMOSFETs. Although, to data, it has never been listed among the electrical characteristics of any data sheet, the parameter does offer important information. We know that JFETs, MOSFETs, and small-signal and power DMOSFETs exhibit current saturation. For the JFET and the depletion-mode MOSFET and DMOSFET, we can identify current

saturation by using the definition I_{DSS}. Not so for the enhancement-mode DMOSFET. Consequently, to know that we can drive the gate to achieve this level of drain current may be important.

Furthermore, we need to be prepared to expect a high $V_{DS(on)}$ [I_{DM} $r_{DS(on)}$] and, in addition, to first check to see whether this possibly unexpected high (calculated) $V_{DS(on)}$ may even exceed our drain potential! If that were true we would be unable to reach the peak current level without first increasing the drain potential.

There are several additional precautions to observe when operating a power DMOSFET at I_{DM} (or, for that matter, at I_D). First and *most important* is not to stray beyond the safe operating region. Second, we need to be aware that the ON resistance of the power DMOSFET will, in all likelihood, exceed the data sheet value because of an effect called the *pinch resistance*.

Pinch resistance results from the close proximity of the channel diffusions of adjacent cells and the resulting depletion regions when a potential exists between source and drain. The equivalent circuit in Figure 5.10 identifies a *JFET* in series with the drain electrode. Comparing the cross-section of a DMOSFET (Figure 1.18) with that of a JFET (Figure 2.1), we see that the DMOSFET channel-depletion field acts very much like the JFET's gate-depletion field, pinching off the flow of current.

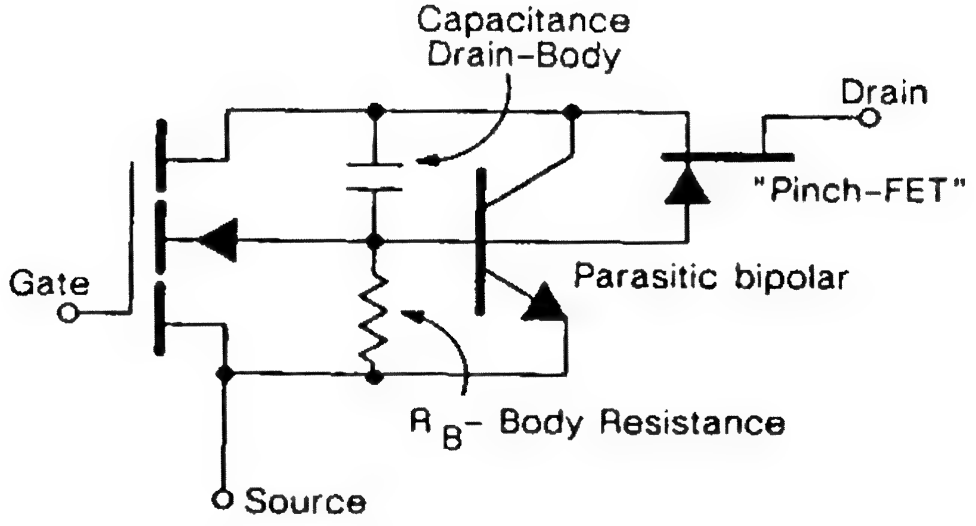

Figure 5.10 Electrical equivalent circuit of the n-channel power DMOSFET. Note the parasitic npn bipolar bridging from drain to source and the "pinch-FET" in series with the drain whose gate is common to the npn base and the DMOSFET body.

5.2.13 I_{DSS} *Zero-Bias Drain Current*

The practical upper current limit for depletion-mode JFETs—provided, of course, that the power rating for the FET has not already been reached—is symbolized by I_{DSS}. Conversely, for enhancement-mode MOSFETs, I_{DSS} identifies the leakage current.

Depletion-Mode JFET

Equation 5.8 and 5.9 coupled with Figure 5.7 identify the tight relation that exists between I_{DSS}, $V_{GS(off)}$, and g_{fs}. Examination of a cross-sectional view of a JFET (Figure 5.6) helps put this into perspective. As the channel beneath the gate enlarges, its capacity to conduct current also increases, its channel resistance decreases (pushing transconductance up), and it takes a greater magnitude of cutoff voltage to effect pinch-off (see Figure 4.4).

Depletion-Mode MOSFET

Unlike the JFET, we are not inhibited from changing the polarity of an unprotected gate (a gate without a protective zener diode clamp). Therefore, I_{DSS} does not represent a current limitation. Instead, our current limitation is *power dissipation.*

Although with depletion-mode FETs the parameter I_{DSS} is often associated with the thought of a maximum saturation current limit, we need to remember that it simply identifies the drain-source current at *zero* gate bias. Once our gate polarity has assumed the polarity of the drain, our depletion-mode MOSFET reverts to enhancement-mode *operation* (but remains a *depletion-mode* MOSFET—remember that I_{DSS}, in this case, is *not* a leakage current). As we further enhance the channel, it is natural to expect a lowering ON resistance and a rising transconductance. Not so! We recognize in light of Eq. 4.7 that to modify the transconductance would require the *ratio* of differential drain current (dI_D) to differential gate voltage (dV_{GS}) to vary. As we saw in Figure 1.10, this does not generally occur. When the MOSFET's transfer characteristic exits the low $V_{GS(off)}$ (or low $V_{GS(th)}$) region, little change occurs. What Figure 1.10 does not show is that when the drain current enters into heavy saturation, the transconductance also saturation

Enhancement-Mode MOSFET

As a leakage current, I_{DSS} identifies the "goodness" of the drain-body, pn, diffusion, and therefore, we find this parameter to be sensitive to the drain voltage, as well as to the chip temperature (see Eqs. 4.3 and 4.4). For power DMOSFETs, this parameter may be characterized to ensure a hard breakdown characteristic. On the other hand, if I_{DSS} is characterized at a drain voltage equal to $V_{(BR)DSS}$, then $V_{(BR)DSS}$ must be characterized at a drain current equal to I_{DSS}! This is covered in Chapter 7.

Although a high level of leakage is generally undesirable, nonetheless, as the I_{DSS} of a power DMOSFET rises, we see a tendency for a swifter minority-carrier recovery, and, therefore, a shorter recovery time, t_{rr}.

Recognizing that this parameter is, in essence, a measurement of the body-drain diode leakage, we should recognize that reverse biasing the MOSFET gate will *not* lower this leakage! There will, of course, be less drain current as we drop the bias below threshold, but only because threshold is established at an arbitrary drain current above that specified as I_{DSS}.

Static-Induction Transistor and Insulated-Gate Bipolar Transistor

Unlike either the conventional JFET or MOSFET, the zero-biased drain current does not define saturation. Since carriers are injected into the channel by virtue of the drain potential, it is insufficient to say that I_{DSS} ($V_{GS} = 0$) alone identifies a presubscribed value of current. A drain potential is necessary, and as we saw in Figure 2.7, a zero-biased drain current is drain-voltage dependent.

Since the IGBT has no drain, the term "I_{DSS}" has no meaning.

5.2.14 I_G *Operating Gate Current*

This parameter is meaningful only when defining the *operating* performance of a JFET. It is this parameter that offers a first-order definition of the d-c gate input resistance according to the equation,

$$R_{in} = \frac{V_{DG}}{I_G} \tag{5.22}$$

5.2.15 I_{GSS} *Gate Reverse Current*

For JFETs and MOSFETs, I_{GSS} identifies leakage in the reverse-biased mode. Often this parameter is used as a first-order definition of the d-c input resistance of the JFET gate. Yet, we must be careful, remembering that this parameter identifies drain and source electrically bonded together, making the test the combined reverse leakage between gate-to-drain and gate-to-source of an *inoperable* FET. Although I_{GSS} may be used as a second-order *approximation* of the d-c input resistance of a JFET, it remains our *only* means of identifying the d-c input resistance of a MOSFET.

5.2.16 I_S *Source Current, or Continuous Reverse Drain Current*

In conjunction at turn-OFF with the rate of decay, dI_S/dt, this parameter plays a critical role in defining the reverse recovery time t_{rr}, of the power DMOSFET.

We see two events related to I_S and dI_S/dt. As the magnitude of I_S varies, it influences the reverse recovery characteristics, as shown in Figure 5.11. As the source-current slew rate (dI_S/dt) becomes more rapid, we find that the reverse recovery *charge* (Q_{rr}) increases while the reverse recovery time (t_{rr}) decreases, as shown in Figure 5.12.

A "step" in the recovery waveform as shown in Figure 5.13 is known as *snap recovery*. If our power DMOSFET is driving an inductive load when this snap recovery occurs, a voltage spike dV_{DS}/dt of extreme proportions may be generated according to the equation:

$$V = L \frac{dI}{dt} \tag{5.23}$$

where L is the inductance in henry, and dI/dt is the slew rate in amperes per second.

A possible result of a snap recovery might be avalanche breakdown or, if the parasitic bipolar transistor becomes activated, a catastrophic second breakdown.

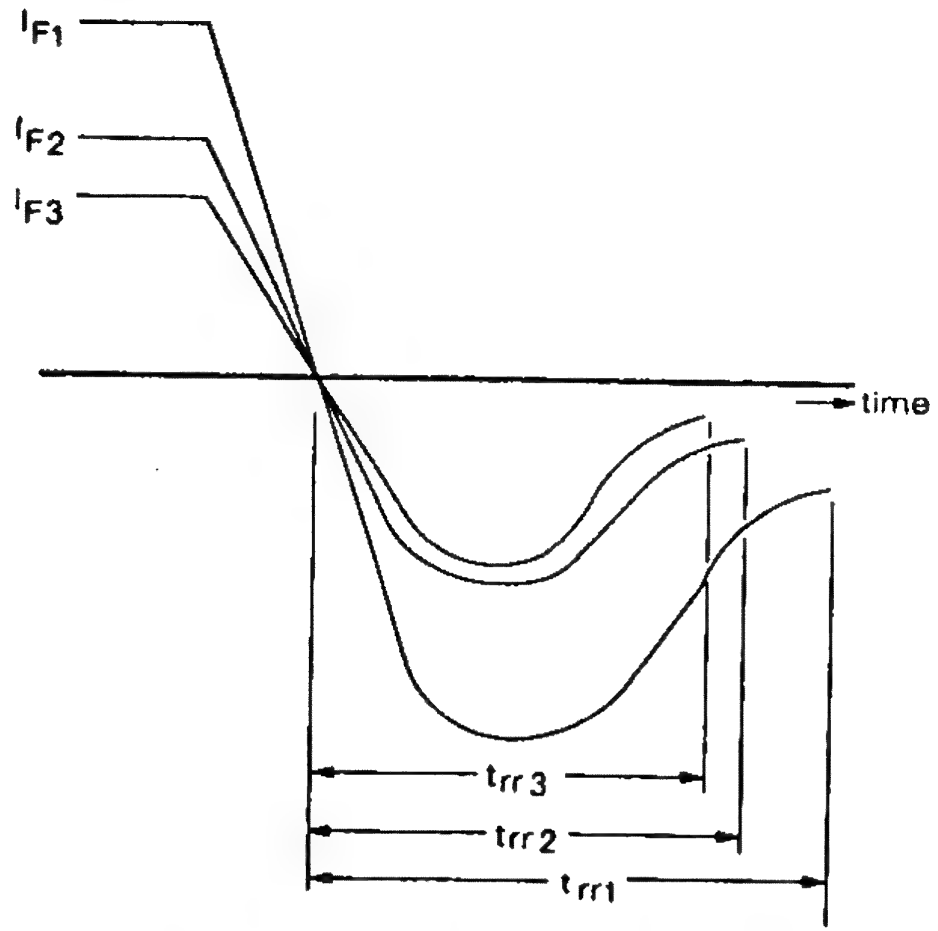

Figure 5.11 Reverse recovery time is directly affected by the magnitude of the source current as well as the slew rate of the current.

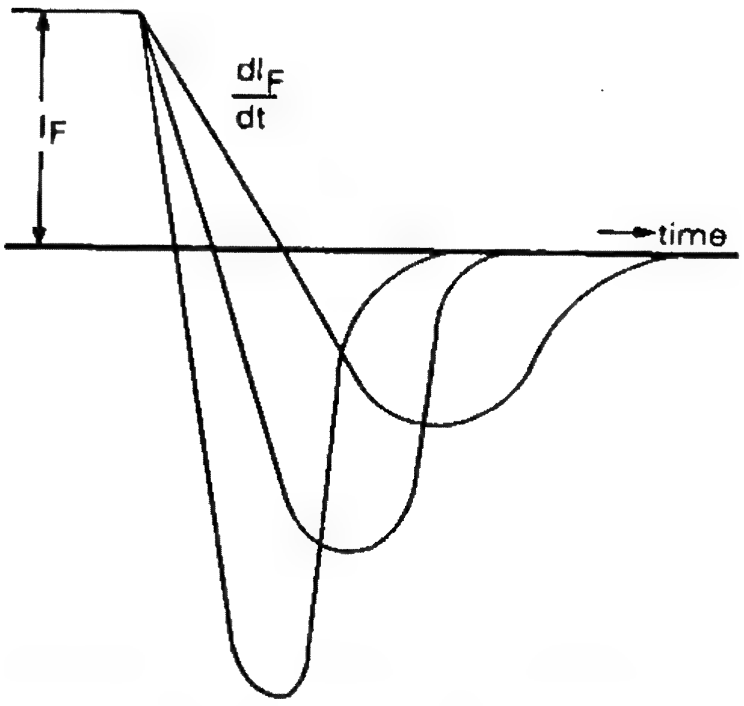

Figure 5.12 As dI_F/dt increases, t_{rr} decreases, but the area within the reverse recovery charge (Q_{rr}) increases.

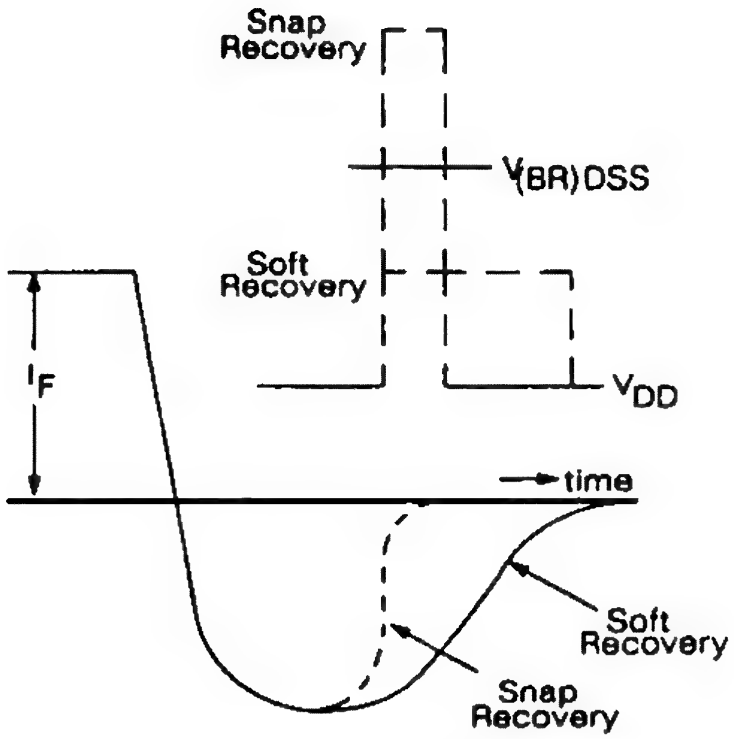

Figure 5.13 Effect of a "snap" recovery on drain voltage.

5.2.17 $r_{DS(on)}$ *Drain-Source ON Resistance*

The $r_{DS(on)}$ affects many parameters regardless of our choice of FET. Regardless of FET type (or style) as $r_{DS(on)}$ diminishes, we see a proportional increase in the FET's capability to handle current. We likewise witness an increase in the parasitic capacitances that encompass the FET. And if we enlarge the geometry to achieve a lower $r_{DS(on)}$, we effect dramatic changes in yield and, therefore, cost.

JFET

The gate-source bias V_{GS}, controls $r_{DS(on)}$. For any particular JFET at $V_{GS} = 0$, we have reached the lowest value of ON resistance, beyond which we cannot go. As the gate bias is manipulated to effect various conditions of $r_{DS(on)}$, we see substantial changes in I_{DSS}, g_{fs}, and g_{os}, and more subtle changes in the parasitic capacitances C_{iss}, C_{oss}, and C_{rss}.

To further decrease $r_{DS(on)}$ we must enlarge the active area. The following offers an example of how the active area relates to $r_{DS(on)}$.

Active area (mm)	$r_{DS(on)}$ (Ω)
0.475 × 0.475	25
0.750 × 0.750	6
1.100 × 1.100	2

As the active area expands, so also does the chip size. As the chip size expands, we improve its thermal resistance and its ability to dissipate heat. What generally limits JFET performance is the header—or transistor package—where the chip is mounted.

Based on what we have learned, it takes little imagination to appreciate that whatever we do to manipulate $r_{DS(on)}$ will also affect many other parameters, in particular, I_{DSS}, g_{fs}, and $V_{GS(off)}$.

MOSFET (Depletion Mode)

Parameter interaction as $r_{DS(on)}$ changes closely emulates that which we experience with the JFET. To lower $r_{DS(on)}$ of a lateral, planar small-signal MOSFET requires widening the channel, since further shortening of the channel is limited by the photolithographic masking techniques. As we widen the channel to further reduce $r_{DS(on)}$, we also affect the threshold voltage, as well as the parasitic gate-channel and gate-substrate capacitance.

SIT

Lowering $r_{DS(on)}$ of a static-induction transistor beyond what can be accomplished with bias is achieved much the same way as for the power DMOSFET. To preserve the breakdown voltage, we parallel cells, enlarging the physical size of the geometry (chip). Adding cells directly affects several parameters such as transconductance g_{fs}, drain current I_D, all the parasitic capacitances, and the thermal resistance θ_{JC}. As the thermal resistance is improved (lowered), the power dissipation of the SIT may improve, if it is not already limited by the header (package).

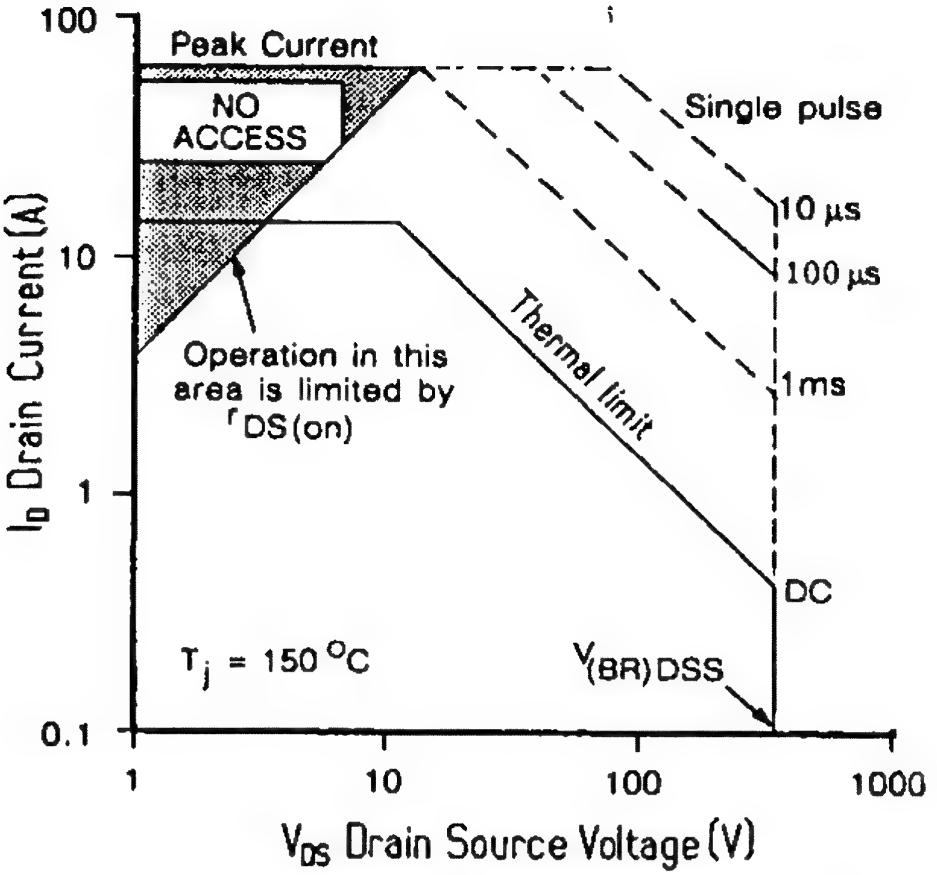

Figure 5.14 The $r_{DS(on)}$ of a power DMOSFET limits its safe operating region.

DMOSFET (Power MOSFET)

As we learned in the discussion accompanying Eq. 4.5, a power DMOSFET cell exhibits a definite relationship between $V_{(BR)DSS}$ and $r_{DS(on)}$. If we wish to lower the ON resistance beyond what we can achieve with bias, we must parallel cells, reaping both the advantages and the disadvantages of a larger geometry.

A major consideration involves the effect of $r_{DS(on)}$ on the safe operating area (SOA)—more correctly, the *active operating area*—especially at lower drain voltages. We must not lose sight of Ohm's law, when studying the SOA of a power DMOSFET (Figure 5.14); $r_{DS(on)}$ limits performance at low drain-source voltages.

A larger geometry at a fixed $V_{(BR)DSS}$ (remember Eq. 4.5) offers a lower thermal resistance R_{thJC}, which, in turn, allows a higher value of drain current I_D (Eq. 3.1), and $I_{D(on)}$. Transconductance increases, the parasitic capacitances increase, and switching times increase (for the same gate drive). A larger geometry often suffers from proportionally higher leakage, I_{DSS}.

5.2.18 $r_{ds(on)}$ *Dynamic ON Resistance*

This parameter affects performance exactly as does the static d-c $r_{DS(on)}$.

5.2.19 R_{thJC} *Thermal Resistance, Junction to Case*

In conjunction with R_{thCS} and R_{thSA} (sink to ambient), which together form R_{thJA}, R_{thJC} forms the basis for determining the power rating of the transistor. As we reduce the thermal resistance, we are able to boost the current rating accordingly.

For the greater majority of silicon junction transistors, the maximum operating chip temperature (T_J) is generally set at 150°C. To operate beyond this temperature may be risky in that few vendors offer guarantees of reliability. The FET, being a majority-carrier semiconductor, is, in essence, a bulk silicon semiconductor whose temperature coefficient is positive. That is, as the temperature rises, so does the ON resistance $r_{DS(on)}$. For small-signal FETs and MOSFETs, the effect of this rise in chip resistance is generally neglected (although it is acutely visible if I_{DSS} is monitored), but for power FETs (SITs and DMOSFETs) the effect is significant. The $r_{DS(on)}$ of some power DMOSFETs rises as much as 2.5 times the value established at 25°C! The effect of temperature on $r_{DS(on)}$ is shown in Figure 5.15.

5.2.20 R_{thCS} *Thermal Resistance, Case to Sink*

As we learned in Chapter 4, this is a user's decision—and an important one, to be sure. Based on our selection of the properly packaged FET, we are able to influence the power-handling capability of a circuit.

5.2.21 R_{thJA} *Thermal Resistance, Junction to Ambient*

The value of this parameter clinches the power performance of the transistor. Regardless of whether our selection is a small-signal JFET or the most massive IGBT, our ultimate power han-

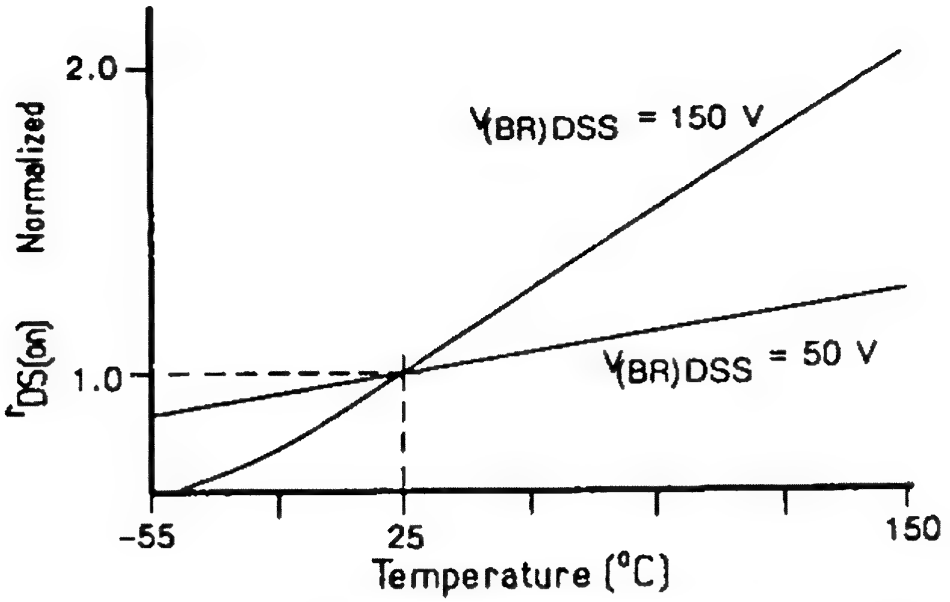

Figure 5.15 Chip temperature effect on $r_{DS(on)}$ for a power DMOSFET also depends on epi resistivity, which, in turn, affects the maximum operating voltage. As the breakdown voltage rises, its effect on $r_{DS(on)}$ becomes more pronounced.

dling depends on how well we have achieved a low thermal resistance from the chip itself (junction) through the heatsink to free, or forced air (ambient). The reader is reminded of the electrical analog of thermal resistance, shown in Figure 3.1.

JFET

If we take a JFET chip measuring 0.580 mm^2, the power dissipation in a TO-52 header is rated at 300 mW. The same chip mounted in a TO-205 header offers a power dissipation of 3 W, an improvement of 10:1!

DMOSFET (Power)

Similarly, if we taken a chip measuring 1.90 mm^2, the power dissipation in a TO-205 header is rated at 6.25 W. The same chip mounted in a TO-204 is rated at 25 W!

As we improve R_{thJA}, raising the power rating, we also improve the current-handling capability according to Eq. 3.1, repeated here for convenience.

$$I_D = \left(\frac{P_D \text{ @ } T_A}{r_{DS(on)} \text{ @ } T_J} \right)^{1/2} \tag{5.24}$$

where the value $r_{DS(on)}$ @ T_J, is obtained from Figure 5.15 by multiplying the normalized value r_N, (the ordinate) by $r_{DS(on)}$ at 25°C, taken directly from the data sheet.

5.2.22 g_{fs} (also as g_m) *Forward Transconductance*

The forward conductance of a FET, measured in Siemens (formerly in mhos), multiplied by the load resistance R_L, in ohms, provides us the *voltage gain* μ. Voltage gain μ (or A_V), multiplied by C_{rss} (C_{gd}) gives the Miller capacitance $C_{in(eq)}$ (see Eq. 4.25). This, in turn, can dramatically alter both the frequency response and the rise time t_r, of the circuit in which the FET is used.

Additionally, in many applications, which we cover in Chapters 9 and 10, the transconductance g_{fs} provides the tools to establish a variety of circuit parameters.

5.2.23 g_{os} *Output Conductance*

The output conductance is the parameter that is identified as contributing to error in voltage gain calculations as well as in constant-current sources. For example, the voltage amplification μ of a JFET may be deduced from:

$$\mu = \frac{e_o}{e_g} = - g_{fs} R_L \tag{5.25}$$

But common as this equation may seem, it does *not* account for high values of output conductance, g_{os}. A more exact equation for voltage amplification is:

$$\mu = \frac{e_o}{e_g} = - g_{fs} \frac{R_L}{1 + g_{os} R_L} \tag{5.26}$$

The importance of knowing the value of g_{os} now becomes glaringly evident. If g_{os} is small compared to $1/R_L$, then Eq. 5.25 offers sufficient accuracy.

Likewise we need to exercise caution when using FETs for constant-current sources, since any change in current is pro-

portional to the product of g_{os} and the change in drain-source voltage (see also Eq. 5.18):

$$dI_D = dV_{DS} g_{os} \tag{5.27}$$

When using FETs where the load resistance R_L, plays an important part in establishing the stage gain and/or bandwidth, the *reciprocal* of g_{os}, r_D, must be considered to be parallel to R_L.

5.2.24 C_{iss} *Common-Source Input Capacitance*

Like all the parasitic capacitances that surround the FET, C_{iss} is a major source of performance degradation. By virtue of its shunting effect, it reduces gain and bandwidth, and because of the additional charge introduced, switching times are slowed.

Perhaps the most insidious parasitic element within C_{iss} is the feedback capacitance C_{gd} (also known as C_{rss}), which, with voltage gain μ, establishes the Miller capacitance $C_{in(eq)}$ (see Eq. 4.24).

A universal equation can be used to define the switching time based on our knowledge of C_{in}:

$$t = R_G \, C \log \left(\frac{V_{GS}}{V_{GS(th)}} \right) \tag{5.28}$$

where

R_G = driving (generator) impedance
C = *total* input capacity, $C_{in(eq)}$

If we consider the FET as an amplifier, this C_{in}, acting as an element of a low-pass filter, will cause the input voltage e_g, to decrease as the frequency increases. A "figure of merit" may be derived that defines an upper frequency limit:

$$f_T = \frac{g_{fs}}{2 \pi C_{in(eq)}} \tag{5.29}$$

The bandwidth (−3 dB rolloff) occurs when the reactance of $C_{in(eq)}$ equals the generator impedance:

$$R_G = \frac{1}{2\ \pi f\ C_{in(eq)}} \tag{5.30}$$

5.2.25 C_{oss} *Output Capacity*

Like its companions, C_{oss} must be accorded its due. In FET switches, it contributes to a phenomenon not unlike the effects of storage time. That is, we see a slowing of the turn-OFF time $t_{d(off)}$, as we wait for C_{oss} to charge back to the rail potential. Of course for a particular FET, if we were to compare this delay to that sustained by the minority-carrier storage time of an equivalent-sized bipolar transistor, we would find the FET to be infinitely faster.

In FET amplifiers for which bandwidth is critical, we need to include this output capacitance as a shunt element in parallel with the load.

5.2.26 C_{rss} *Reverse Transfer Capacitance*

Otherwise known as C_{gd}, the parameter C_{rss} is, of all the parasitic capacitances, the principal cause of performance degradation. In switching applications it contributes not only to the Miller effect (see Section 5.2.24), but to a phenomenon called *charge injection*.

The charge transferred from gate to load, common in JFET sample and hold circuits (generally a holding capacitor), is given by:

$$dQ = dV\ C_H \tag{5.31}$$

where

dQ = charge transferred between gate and load capacitance C_H
dV = resulting error voltage

The charge-transfer characteristics dQ vary considerably depending on the type of FET and the circuit used. Every com-

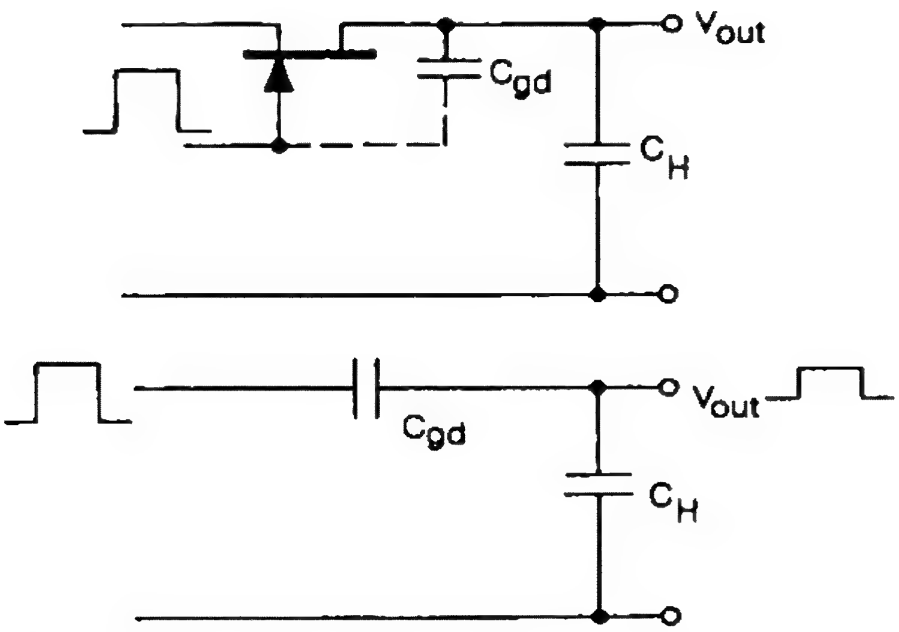

Figure 5.16 Gate-to-drain capacity C_{gd}, forms a voltage divider network with the holding capacitor C_H in any sample and hold circuit.

bination must be measured. A simplistic equivalent circuit appears as a capacitive voltage divider consisting of C_{gd} and C_H (see Figure 5.16). CMOS switches (the combination of complementary n- and p-channel MOSFETs) offer a major advantage in combating charge transfer. Whatever charge is injected when the n-channel MOSFET is switched is (theoretically) removed by the p-channel MOSFET. This is somewhat visible in Figure 5.17.

In amplifier applications, C_{rss} contribution to the Miller capacitance severely limits the gain bandwidth (GBW). For example, let us calculate the GBW of two FETs, both having a forward transconductance g_{fs}, of 14 mS and C_{gs} of 4.9 pF. The JFET has a C_{gd} of 1.2 pF, whereas the other FET (a dual-gate MOSFET, or a pair of cascaded FETs) has a C_{gd} of 0.2 pF:

$$GBW = \frac{g_{fs}}{2\,\pi(C_{in(eq)})} \tag{5.32}$$

Solving for $C_{in(eq)}$ using Eq. 4.24, we use Eq. 5.32 to solve for GBW:

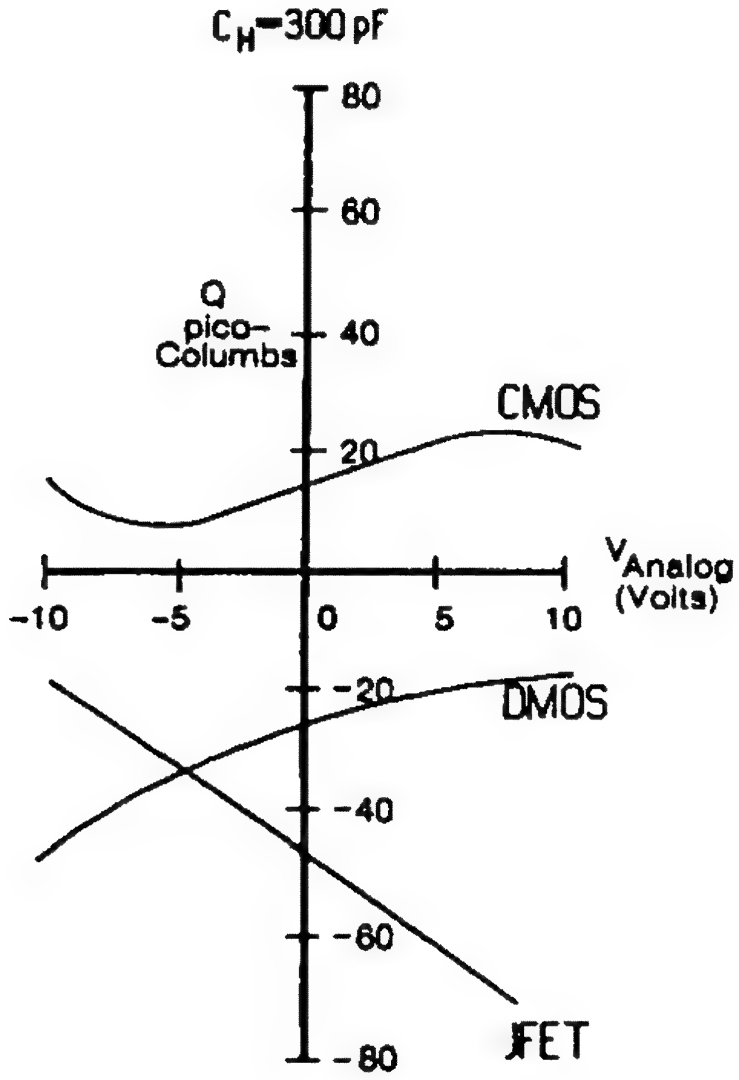

Figure 5.17 A comparison of charge coupling between JFET, CMOS, and DMOS analog switches. Charge coupling is difficult to quantify without making actual measurements because of the many hard-to-define variables.

C_{gd}	GBW
1.2 pF	50 MHz
0.2 pF	485 MHz

5.2.27 $t_{d(on)}$ *Turn-ON Delay Time*

Not only does $t_{d(on)}$ affect performance, but because of the depletion-dependent nature of the parasitic capacitances, as the gate-to-source potential changes, so does the gate-to-source capacitance. Before the FET actually begins its turn-ON cycle,

during the interval of $t_{d(on)}$, the gate charge brings the potential across the input capacitance C_{gs}, to a point at which the gate is able to exert control. During this interlude the FET is inoperable and all parameters are static.

5.2.28 t_r *Rise Time*

Rise time indirectly affects other parameters, as well as, of course, performance. As the drain-source voltage collapses toward V_{SAT}, both C_{iss} and C_{oss} increase as the depletion fields collapse. As the drain current rises in magnitude, followed by the voltage gain μ, the Miller capacitance (Eq. 4.24) becomes predominant.

We also need to accept an obvious conclusion: turn-ON time is not an instantaneous step function. Switching losses occur during this phase. For purely resistive loads, the loss is simply $I_{D(rms)}{}^2 r_{DS(on)}$. But for reactive loads, such as relays, motors, and transformers, the power factor contributes to additional switching losses within the FET, as we see in Figure 5.18. The fact that power is lost in the transistor demonstrates that efficiency is also dependent on t_r.

Depending on the power involved (magnitude of current and voltage, switching time, and duty cycle), t_r may be detrimental to the safe operating area (SOA).

Small FETs (rated at 1 W or less) seldom are specified with respect to SOA. Our only clue to mistreatment may be an unex-

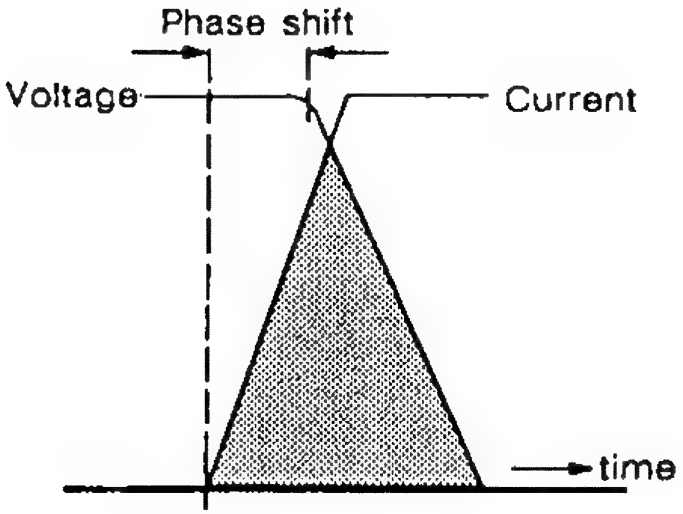

Figure 5.18 The effect of power factor on the internal switching losses of a power FET.

pected—and possibly unnoticed—temperature rise leading to premature or sudden failure.

5.2.29 $t_{d(off)}$ *Turn-OFF Delay Time*

Nowhere as long as minority-carrier storage time of a similarly rated bipolar transistor, $t_{d(off)}$ identifies the time the FET remains ON, consuming power and increasing its junction temperature, until V_{GG} once again takes control of the gating action to begin the process of shutdown. As before, we find that the parasitic capacitances do not stand still as the gate-source voltage moves.

5.2.30 t_f *Fall Time*

This parameter restores the FET to its original nonconducting state with full drain voltage impressed and no current, other than leakage current, passing between drain and source.

As we witnessed with rise time, because of the rapidly changing drain current dI_D, the Miller effect predominates (see Eq. 4.24), greatly affecting $C_{in(eq)}$.

5.2.31 t_{rr} *Reverse Recovery Time*

The time that reverse current is passing through the body-drain diode of the power DMOSFET is represented by t_{rr}. Because of the characteristically slow diode recovery, in many applications involving more than one DMOSFET, we may experience excessive power dissipation, and possible destructive current spiking at higher switching frequencies.

5.2.32 Q *Charge*

In essence, the charge Q is what makes the FET work. As we alter charge, we alter current. Change the charge on the gate, and the drain current follows suit. Change the charge in the body-drain diode during reverse recovery, and we change the reverse recovery time. Even the *transit time* of the semiconductor is influenced by charge. Charge plays a critical role in

the switching time. Equation 5.28 could be rewritten to reflect the more universal influence of charge:

$$t = R_G \left[\frac{Q}{V}\right] \log\left(\frac{V_{GS}}{V_{GS(th)}}\right) \qquad (5.33)$$

5.2.33 $Q_{g(th)}$ *Gate Threshold Charge*

This parameter and C_{gs} can be in disagreement despite Eq. 4.23 (and Figure 4.26) simply because C_{gs} reflects *all* the gate-source capacity including both active and passive, whereas $Q_{g(th)}$ should identify *only* the contribution of active capacitance: the capacitance that contributes to device operation.

5.2.34 $Q_{g(on)}$ *Gate Turn-ON Charge*

We use $Q_{g(on)}$ to bring the DMOSFET to full ON. The drain-source voltage V_{DS} equals $V_{DS(on)}$, or V_{SAT}.

5.2.35 dV/dt (Mode 3)

The parameter dV/dt occurs as a *dynamic* test of the power DMOSFET when the body-drain diode is at its peak of current conduction, a fast slew drain voltage forces this diode current (collector-base current) to bias the parasitic bipolar transistor into conduction. Since BV_{CEO} (of the bipolar) is much less than $V_{(BR)DSS}$, burnout occurs.

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6

Thermal Relationships
and Their Impact Upon Performance

6.1 Introduction

The principal cause of failure of any transistor is excessive heat. Regardless of the size of our FET, if we are careless in our understanding of its thermal characteristics, a blunder may soon result in catastrophic failure!

Nearly all the characteristics of FETs (with the notable exception of their parasitic capacitances and switching times) are sensitive to the internal junction temperature of the device. Since the electrical characteristics, or data sheet ratings, are merely design limits, they too depend on the junction temperature.

Despite observations that may appear to contradict this statement, the *bulk* resistance of all FETs has a positive temperature coefficient with respect to $r_{DS(on)}$. That is, as the junction temperature rises, $r_{DS(on)}$ also rises. If, in our application, we inadvertently or otherwise have the drain current I_D, under the control of external influences (a current source or an inductor), we will more than likely force a regenerative thermal effect, popularity known as thermal runaway. For small-signal JFETs and MOSFETs this regenerative effect may be less dramatic than it would be with a power FET.

To bring the temperature problem close to home, let us consider two common exercises: first, the examination of I_{DSS} of a small-signal JFET; second, an attempt at confirming the $r_{DS(on)}$ of a power DMOSFET.

The easiest solution for both exercises is to use the Tektronix curve-tracing oscilloscope, which allows both static and pulsed measurements. Suppose, however, that in our haste we commit two fundamental errors: since pulsed measurements are more arduous to see, we (1) choose the static mode and (2) fail to attach a suitable heatsink to either FET case.

What happens when we try to measure I_{DSS} of the small-signal JFET? We may see the output characteristics drift downward across the scope. Any guess as to the value of I_{DSS} would be just that—a guess.

What happens when we try measuring $r_{DS(on)}$ of a power DMOSFET? There is an excellent chance that the measured value will exceed the data sheet specification.

These scenarios are, of course, superficial, but they illustrate frequently perpetrated errors. In both situations there was failure to appreciate the effect of chip temperature T_j, on $r_{DS(on)}$ (see Figure 5.15). As the chip temperature rises, conduction losses ($I_D{}^2 r_{DS(on)}$) rise, which, in turn, increases the chip temperature. A regenerative runaway cycle begins.

Data sheets provide electrical characteristics at either 25°C case (T_C) or ambient (T_A) temperature. *Only when the FET is operated at the prescribed temperature will it meet the data sheet specifications.* Therefore—if we wish our FET to perform as we have every right to expect—we need to thoroughly understand the thermal requirements and the methods of heatsinking.

6.2 Are Heatsinks Necessary?

In some instances, perhaps not. However, before we draw that conclusion, we must evaluate each situation. Without a doubt the singular cause of semiconductor failure is the generation of excessive junction heat. In our quest for long-term reliability, studies have established a maximum junction temperature $T_{j(max)}$ of silicon in the vicinity of 150°C; for germanium, $T_{j(max)}$ is 80°C. These, of course, are not absolutes: some manufacturers have rated silicon power devices at 175 to 200°C, and germanium power devices to 100°C.

A rule of thumb suggests that every 10°C rise beyond the maximum safe T_j reduces the life expectancy of the device by 50%!

Any good semiconductor data sheet will offer, with the power rating, either a thermal resistance specification R_{thJC}, or a thermal (power) derating specification. Thermal resistance may

be identified by the dimension—degrees Celsius per watt (°C/W). Thermal derating is the *reciprocal* (W/°C). Small-signal FETs may have either the thermal resistance or derating factor in *milliwatts* (mW). A FET with a thermal resistance R_{thJC}, of 5°C/W has a derating factor of 0.2 W/°C, and if it dissipates 5 W, its junction temperature is 5 × 5 = 25°C *above* its case. The equation for the junction temperature is:

$$T_j = [P_{diss} R_{thJC}] + T_C \tag{6.1}$$

If we fix the maximum operating temperature $T_{j(max)}$, at 150°C, the derating factor, D.F., identifies a maximum power dissipation of 25 W at a case temperature T_C, of 25°C:

$$P_{diss} (@ T_C) = (T_{j(max)} - T_C)D.F. \tag{6.2}$$

6.2.1 How Do We Answer the Question?

We first need to establish the maximum operating temperature of the FET. That parameter is supplied by the vendor and is usually found on the data sheet under the column labeled "Absolute Maximum Ratings" as one of the following:

Maximum operating temperature
Operating temperature range
Operating junction and storage temperature range

Generally, for silicon, we should expect to see temperatures ranging from 150 to 200°C.

Next, we search for the power rating of the package. In the same column, this should be offered as "Total device dissipation at T_X = 25°C."

It is important to note if the temperature is specified either as "free air," more properly known as ambient (T_A), or as case (T_C), with this rating should be a power derating specification (the word "power" may be omitted).

In Chapter 5 we compared the performance of a depletion-mode, small-signal FET (JFET) chip measuring 0.580 mm^2 packaged in a TO-52 header with a power rating of 300 mW and in a TO-205 header with a power rating of 3W.

An overly cautious first step might be to question the ratings themselves. How can we be sure that the TO-52 header will dissipate 300 mW in an ambient environment (T_A) of 25°C?

We can measure it! There are a variety of methods, some quite sophisticated, some not. All we need for the latter is a curve-tracing oscilloscope, a temperature-controlled oven, and a single well-founded assumption.

Our assumption is that when *pulsing* a zero-biased JFET at I_{DSS}, insignificant power is dissipated in the chip. If this is true (and we assume that it is), then the junction temperature T_j, equals the case temperature T_C, and also equals the ambient T_A, so we have:

$$T_j = T_C = T_A \tag{6.3}$$

Small-Signal FETs

A JFET exhibits a negative temperature coefficient, meaning that as T_j rises, I_{DSS} drops. Conversely, we may say that a JFET (indeed, *any* FET) exhibits a positive temperature coefficient for $r_{DS(on)}$, which rises with increasing temperature. By placing the JFET in the oven and monitoring I_{DSS} as we increase the temperature, we can plot the change in I_{DSS}, as we show in Figure 6.1.

Armed with this information, we have what we can label as a temperature-sensitive parameter (TSP) for that particular geometry. That is, we can now measure I_{DSS} and *know* the junction temperature T_j, irrespective of either ambient or case temperature! However, since we are looking for a confirmation of the JFET's total device dissipation, it is important to reduce the likelihood of either conduction or convection cooling during the tests to be described.

Having calibrated the TSP of our FET, we begin with the oven (and JFET) at 25°C, but we no longer pulse our test. Rather, I_{DSS} is measured in the steady state. With $|V_{DS}| > |V_{GS(off)}|$, when I_{DSS} stops its downward drift we can identify T_j, as we show in Figure 6.1.

Quite likely in this exercise our value of T_j may be less than the rated maximum operating temperature. To firmly establish the maximum power dissipation, we need only adjust our V_{DS} upward—while *carefully* monitoring I_{DSS}—until $T_{j(max)}$ is reached. At that moment, our maximum power dissipation (at $T_{j(max)}$) is simply:

$$P_{Diss(max)} = I_{DSS} V_{DS} \tag{6.4}$$

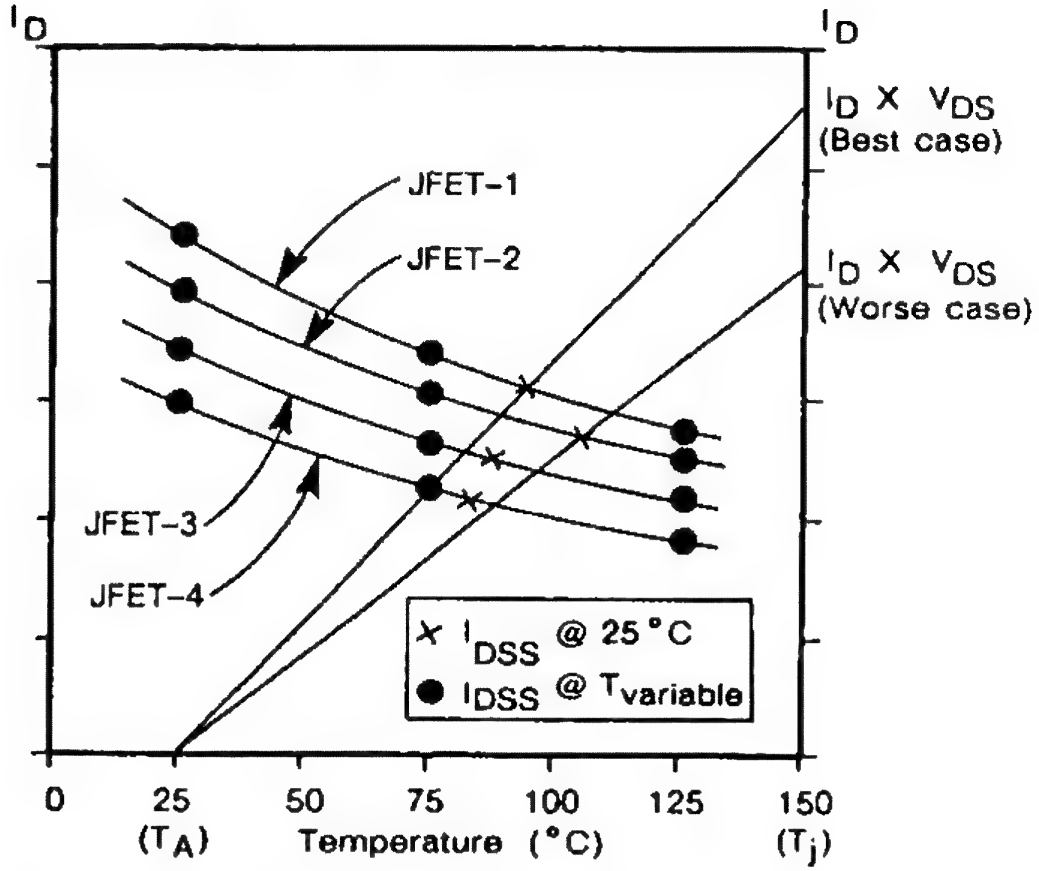


Figure 5.1 The drain saturation current I_{DSS}, as a temperature-sensitive parameter (TSP) becomes the principal tool in determining the thermal characteristics of the JFET. The smooth curves show the effect of temperature on pulsed I_{DSS}. Crosses identify the measured I_{DSS} under power, from which the respective junction temperatures are easily read.

Some JFETs may have a high value of g_{os} that would cause the measured value of I_{DSS} to rise with a rising V_{DS}, which would tend to introduce error into Eq. 6.4. In that case we need only extrapolate the measured data as shown. An ordinate, calibrated in I_D, rising at $T_{j(max)}$, intersected by a straight-line projection originating at T_A = 25°C and passing through the measured value of I_{DSS}, provides the value of I_D used in the simple equation for maximum power dissipation:

$$P_{Diss(max)} = I_D \, V_{DS} / T_j = K \tag{6.5}$$

The manufacturer of this JFET further claims that when packaged in a TO-205, 3 W dissipation is guaranteed if the case is held at 25°C.

Those experienced in the art may appreciate that this is easier said than done. The difficulty of making the measurements above with the JFET firmly embedded in a 25°C heatsink is compounded by the continual flow of heat from the JFET case to the heatsink. In all likelihood, the heatsink temperature in the immediate vicinity of the JFET case will *not* remain at 25°C without special effort on our part (notwithstanding that for all JFETs mounted in the TO-205, the gate connection is the case, which requires us to electrically isolate the heatsink).

To succeed in this task we place a small (no. 30 AWG) thermocouple on the surface of the header between the leads, to be directly beneath the chip. Operating at I_{DSS} we read the temperature measured by the thermocouple and extrapolate to I_D as described above (for Figure 6.1). We assume the thermal resistance to be constant and scale upward (the opposite of derate) the device performance to 25°C.

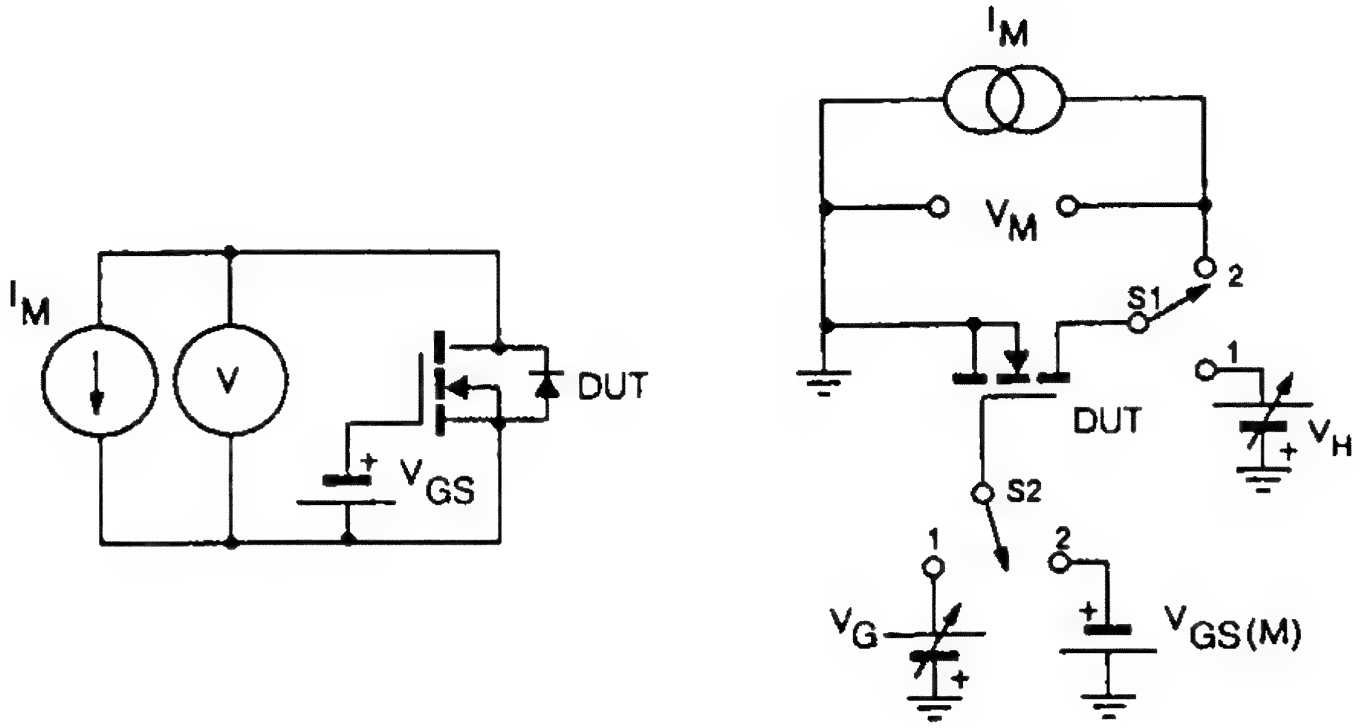
Power DMOSFETs

Enhancement-mode FETs, such as power DMOSFETs, may be characterized similarly. As before, we need to establish a TSP, or K-factor. For the power DMOSFET the body-drain diode is the likely candidate and the calibration procedure follows that for I_{DSS}, except, of course, we measure the forward diode voltage V_{SD}, instead, at a low I_S current of a few milliamperes.

The magnitude of this diode current must be such that the diode is ON; furthermore as we span the temperature range (25 to -150°C) V_{SD} must decrease *linearly* with increasing temperature.

With the case well heatsinked and a thermocouple placed on the base of the header central to the chip location, we pulse the drain current—heating the chip while current flows—and measure V_{SD} (diode forward voltage) when the current is OFF. Since the diode has been calibrated (our TSP), we are able to determine the chip temperature. The procedure is a bit complicated, as shown in Figure 6.2, and often requires some advanced test equipment. Monitoring the case temperature with the thermocouple and the chip temperature with the calibrated body-drain diode and knowing the d-c power (V_{DS} I_D), we can scale upward to determine the maximum power dissipation at T_C = 25°C.

The slope of our derating curve represents the linear derating factor; its reciprocal is the thermal resistance R_{thJC}.



(a) (b)

Figure 6.2 (a) The K-factor calibration setup, and (b) a thermal impedance measurement circuit using the "source-drain" method from MIL-STD-750C, Method 3161. Both tests are easily performed using the Sage model 230, 235, and 240 Star systems.

At this point we know, or have confirmed, the following for the small-signal FET:

Maximum junction temperature, $T_{j(max)}$
Maximum power dissipation at $T_A = 25°C$
Thermal resistance, chip to case, R_{thJC}
Linear derating factor

Our confirmation of the power DMOSFET includes the above but modified to show maximum power dissipation at $T_C = 25°C$.

If we plan to use this 300 mW JFET at power levels under 300 mW at ambient room temperatures, we will not need a heat-sink. On the other hand, if we plan to operate at elevated temperatures, we need to refer to the linear derating factor to determine our maximum free-air power limit. This may also be expressed as follows:

$$T_{j(max)} = P_{(max)} R_{thJC} + T_A \qquad (6.6)$$

or

$$P_{(max)} @ T_A = \frac{T_{j(max)} - T_A}{R_{thJC}} \quad (6.7)$$

But what if we wish to operate at a power level higher than what Eq. 6.7 allows? The answer is obvious: we need a heatsink.

Our problem with the power DMOSFET is more complicated, since it is rated at a *case temperature*, T_C, of 25°C. Immediately we sense that a heatsink is necessary unless we were able to operate at considerably reduced power levels. With power transistors rated at T_C, we may substitute T_C for T_A in Eqs. 6.6 and 6.7.

6.2.2 What Size Heatsink?

If we wish to operate at power levels higher than the transistor allows, we must remove as much heat from the junction as possible. The sole function of the heatsink is to lower R_{thCA}—the thermal resistance between case and ambient.

Using a heatsink modifies Eq. 6.7 as follows:

$$P_{(max)} @ T_A = \frac{T_{j(max)} - T_A}{R_{thJC} + R_{thCA}} \quad (6.8)$$

where R_{thCA} includes the thermal resistance of the heatsink.

$$R_{thCA} = R_{thCS} + R_{thSA} \quad (6.9)$$

This equation emphasizes the importance of *knowing* the thermal resistance of a heatsink. We do not just pick up any heatsink; we select the right heatsink for the job. A useful guesstimate of thermal efficiency of a finned heatsink that relies solely on natural convection cooling is provided in Figure 6.3. Of course, once our ambient temperature has reached the maximum operating temperature of the junction, $T_{j(max)}$, no heatsink can help; our derating factor has reduced our maximum power to zero!

If our application demands higher ambient temperatures, we can judiciously raise our value for $T_{j(max)}$, and, using the

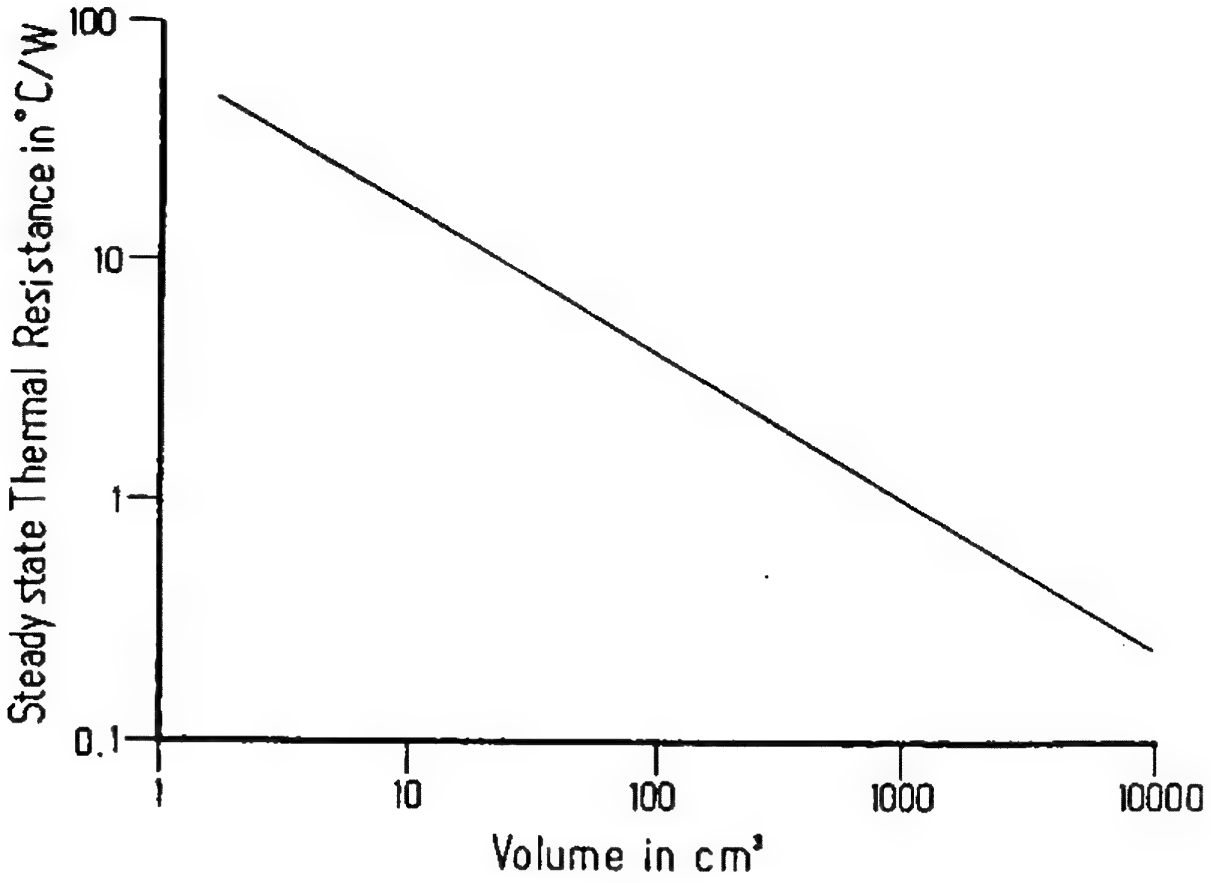


Figure 6.3 Steady-state thermal resistance of a finned heatsink in still air.

equations, derive new thermal characteristics. But unless special precautions were undertaken by the vendor, such experimentation may shorten the lifetime of the transistor. Studies show that the maximum allowable die temperature is inversely related to contaminants resident within the semiconductor. Contaminants migrate at a rate determined by temperature and applied voltage. A useful test to determine the suitability of operating at temperatures above the normal data sheet rating would be to subject the FET to a high-temperature reverse (gate) bias test (HTRB). Equipment users are cautioned to *always* obtain a reliability report from the vendor before subjecting FETs to operating temperatures higher than those specified on the data sheet.

6.3 Safe Operating Area

The safe operating area (SOA), presented graphically, has been the mainstay of the power bipolar transistor for years. More

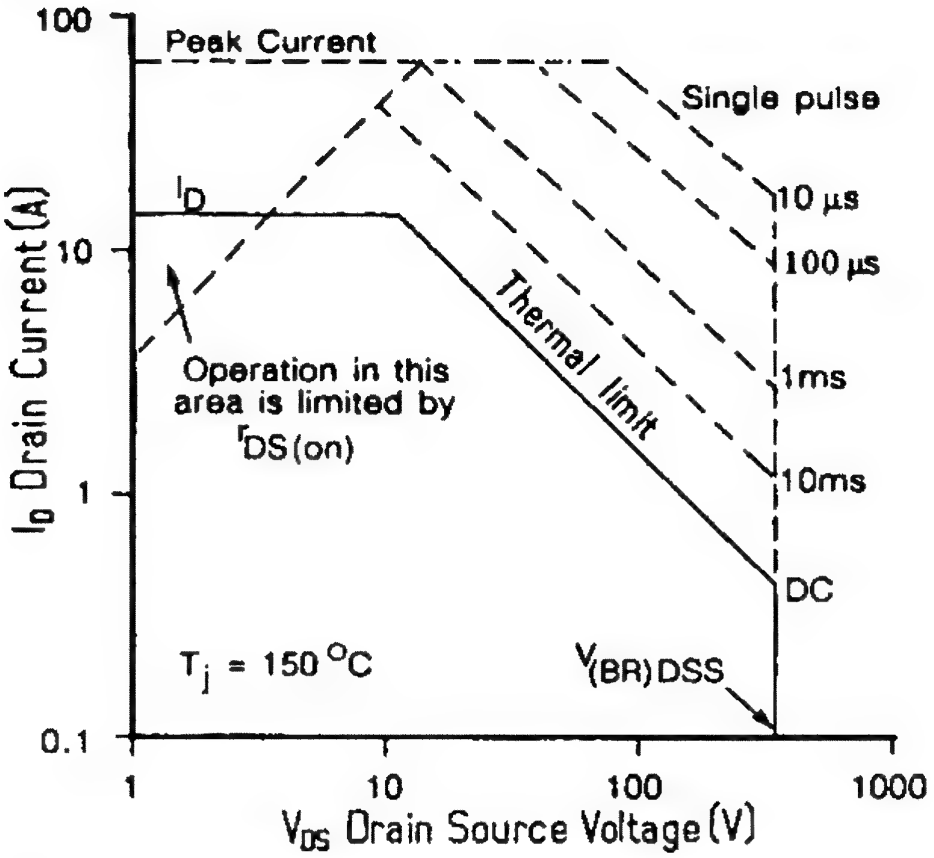


Figure 6.4 Safe operating area of the typical power DMOSFET is bounded by three dimensions: breakdown $V_{(BR)DSS}$, power dissipation (or thermal limit), and peak current. A more insidious limit is $r_{DS(on)}$, which affects the minimum V_{SAT}.

recently we have seen the SOA curve on power FET data sheets. Although we may feel more comfortable having these data at hand, we must not lose sight of the fact that the SOA data apply only to a *single pulse*! The SOA itself does not represent a steady-state condition. If we plan to use the power FET in other than a one-shot, pulse-driven application, the SOA data will offer little comfort.

Unlike the SOA of the power bipolar transistor, the power DMOSFET's SOA (Figure 6.4) identifies a few interesting anomalies: (1) no second breakdown and (2) if compared with an equivalent-rated power bipolar transistor, the FET offers a higher pulse power capability.

The safe operating area curves are derived from the transient thermal impedance curves for a single pulse.

6.4 Transient Thermal Impedance

In Figure 3.1, we presented a simplified electrical analog for a FET operating in the steady state. Using the parameters offered in this figure, we can determine the operating chip temperature T_j:

$$T_j = T_A + (R_{thJC} + R_{thCS} + R_{thSA})P_T \tag{6.10}$$

The series enclosed by parentheses can be further simplified to reflect the total *junction-to-ambient* thermal resistance:

$$R_{thJA} = R_{thJC} + R_{thCS} + R_{thSA} \tag{6.11}$$

Therefore,

$$T_j = T_A + (R_{thJA})P_T \tag{6.12}$$

where P_T is the total power dissipated by the FET.

Equation 6.12 is, for all intents, identical to Eq. 6.1, if we substitute T_C for T_A.

It is not difficult to envision the means by which the transient thermal impedance curve (Figure 6.5) is generated. The

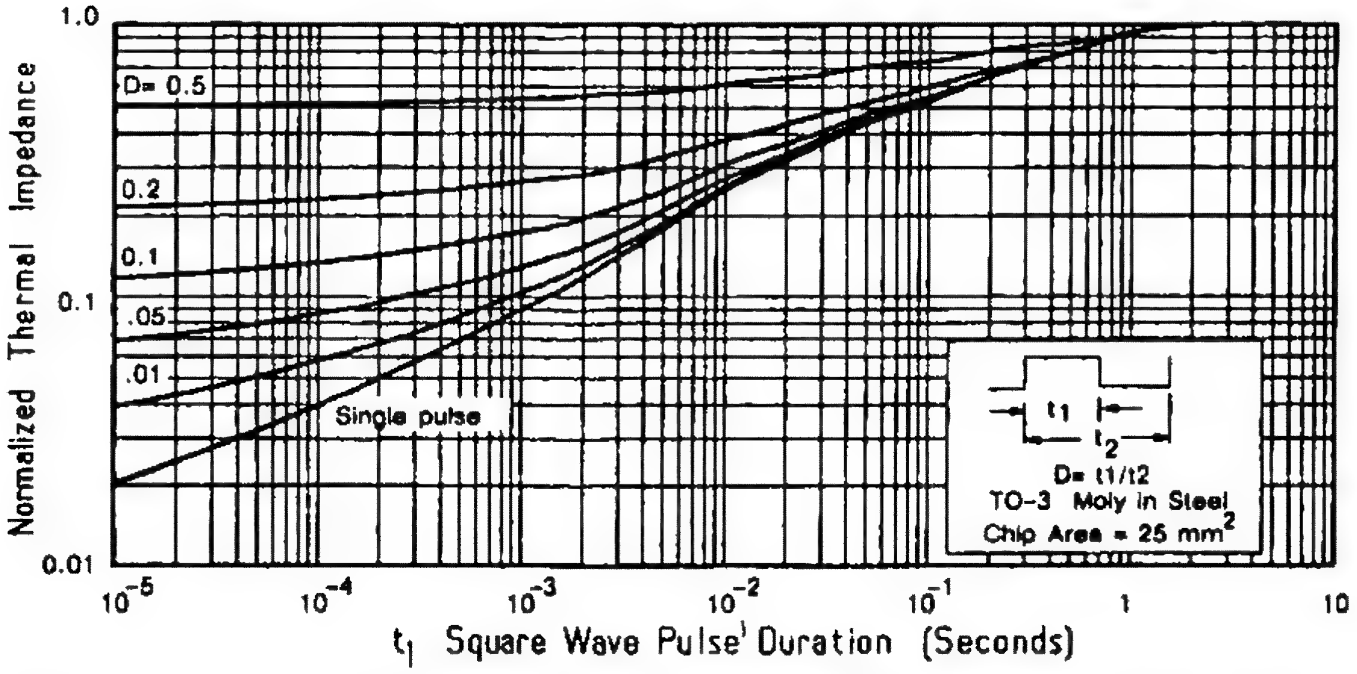


Figure 6.5 Transient thermal impedance depends on chip area, the thermal resistance of the header, and the applied power duty cycle.

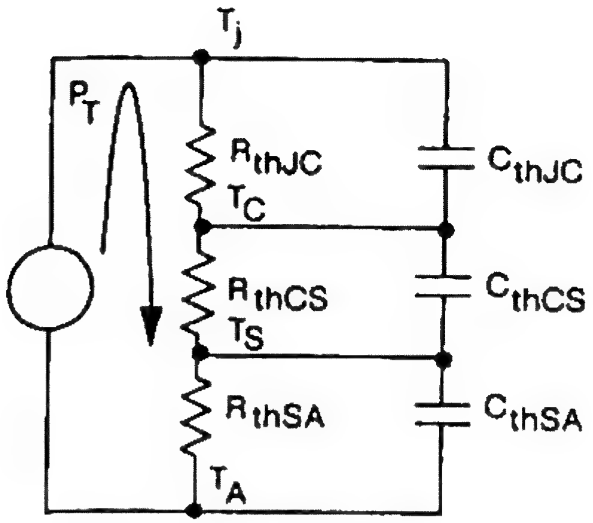


Figure 6.6 Simplified thermal analog with capacitors representing the thermal mass of each element.

power transistor has mass, to which each element in the transistor contributes: the semiconductor chip, the case (or header), and the heatsink, if one is used. Each component of mass has a thermal response; it takes a finite time to absorb—and dissipate—heat. We can use the analogy by adding to Figure 3.1 a series of capacitors representing this mass, as shown in Figure 6.6.

If we were to turn on the power FET, we would expect the chip temperature to rise to an operating level in a finite amount of time t. In Figure 6.7, this is shown to be the steady-state level. However, if we turned the FET off after a short interval (milliseconds), we would also expect to see a thermal decay (dissipation), depending on the storage capacity of the individual elements. This is also illustrated in Figure 6.7. We expect T_j to rise proportionally to the peak power applied, and to the length of time the power was applied (t_p).

Whereas before we were involved in power ratings, thermal resistances, and derating factors, we now have added a new dimension—a *time*-dependent factor r(t).

To account for thermal capacity, this time-dependent factor must be applied to the steady-state thermal resistance:

$$R_{thJC(t)} = r(t)\ R_{thJC} \qquad (6.13)$$

For very short pulses of power r(t) is small; but as the length of time the power is applied (pulse width—t_p) is increased, r(t) approaches unity. At unity, the transient thermal resistance

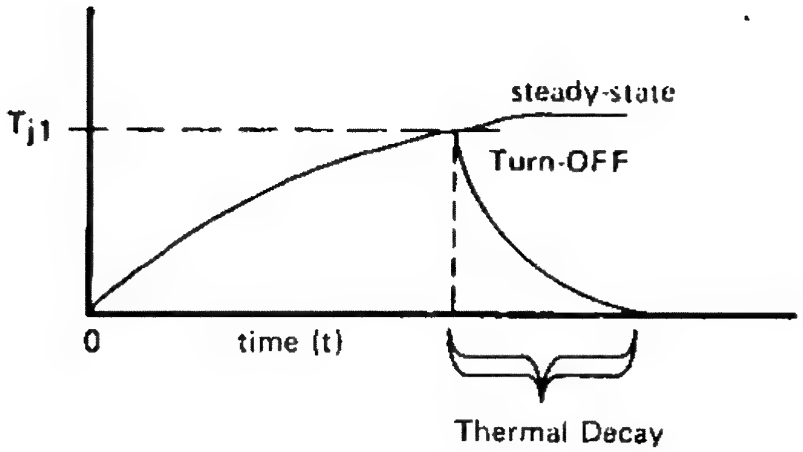


Figure 6.7 Temperature buildup and subsequent thermal decay for *one* power cycle.

equals the steady-state value and Figure 6.5 begins to become believable.

To this point our concern has centered on a single pulse. Most applications are not that simple. Fortunately the transient thermal impedance curve provides for repetitive pulses. The duty factor D is:

$$D = \frac{t_p}{T} \tag{6.14}$$

6.4.1 Using the Transient Thermal Impedance Data

Some conditions must be recognized as having prevailed as we studied Figure 6.5. Perhaps the most fundamental is that we assumed our pulse to be rectangular. Regrettably, that condition seldom occurs.

Handling Nonrectangular Power Pulses

Rather than delve into complex wave analysis, we can make simple approximations to achieve reasonable solutions.

1. For a pulse that is nearly rectangular, we let the amplitude remain but adjust the width to equalize the energy. That is, we maintain equal area.

2. Sine wave and triangular power pulses may be modeled by setting the amplitude at 70% of the peak and the width to

91% of the baseline width for the sine wave and 71% for the triangular wave.

For more complicated power pulse waveshapes, the reader is encouraged to consult the references concluding the chapter.

References

Roehr, Bill, and Shiner, Bryce (1972). "Transient Thermal Resistance—General Data and Its Use," Applications Note AN-569, Motorola, Inc., Phoenix.

Roehr, Bill (1973). "Mounting Techiques for Metal Packaged Power Semiconductors," Applications Note AN-599, Motorola, Inc., Phoenix.

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Siegal, Bernard S. (1985). *Thermal Characterization and Die Attachment Evaluation of Semiconductor Devices*, Sage Enterprises, Inc., Mountain View, CA.

Siliconix inc. (1984). Safe Operating Area and Thermal Design for MOSPOWER Transistors (AN83-10). In *MOSPOWER Applications Handbook*, Siliconix inc., Santa Clara, CA.

7

How to Read a Data Sheet
and Understand What You Are Reading

7.1 Introduction

If you have ever used a FET and found that it does not perform as expected, perhaps you misread the data sheet. Of course, you may have read the data sheet correctly; perhaps you disobeyed the design rules. In either case, you probably should reexamine the data sheet.

On the other hand, quite likely you are concerned that the performance of the FET you are using appears to differ from that of others you have used having the same part number. There are at least two probable reasons for this. First, take careful note of the data sheet parameters: they are anything but tight. Many FET data sheets offer wide-ranging values of either $V_{GS(off)}$ or $V_{GS(th)}$, both of which are critical parameters for establishing performance. Second, FETs from different manufacturers may differ in performance. All we should expect is that the FET perform within the limits of the data sheet.

Once you realize that the data sheet is a form of advertising (and there are no laws regulating truth in advertising for data sheets), you may (and should) be on your guard. For example, if the ubiquitous IRF230, fabricated by at least four manufacturers, were exactly the same from each, what would be the incentive to buy from any one vendor, aside from price and delivery? Yet, you may say that if a device meets the data sheet specifications, all samples of it *should* be identical. Not so. Perhaps the data sheet offers leeway for significant variation

between vendors. What then is your strategy to assure yourself that you have the best product for a particular application?

An interesting exercise would be to open these four IRF230s and compare the semiconductor geometry in each header. You might not need a microscope to see dramatic physical differences!

On the other hand, do not be misled thinking that a JEDEC-registered data sheet (2N####) offers security against troublesome specifications. The committee that issues registration has no policing power. Your best insurance is to know what specifications are important. Then determine whether they have been adequately identified on the data sheet and, if you have any questions, ask the vendor.

This chapter does *not* lead you through every facet of the data sheet. The sole intent of this chapter is to acquaint you you with data sheet specifications that may not be entirely what they at first seem to be.

7.2 Pitfalls and Dilemmas

We have covered several varieties of FETs, and since their data sheets are too dissimilar to allow direct comparison, we must focus on each type of FET.

7.2.1 Scrutinizing the Small-Signal JFET Data Sheet

There are three basic data sheet formats that identify the JFET's intended application:

1. The switching JFET (Figure 7.1)
2. The amplifier JFET (Figure 7.2)
3. The differential-pair JFET (Figure 7.3)

We can give each of these data sheets cursory examination to discover the intended application. By comparing Figures 7.1 and 7.2 we see the obvious. The switching JFET data sheet for the 2N4391 series offers several parameters not found on the amplifier JFET data sheet. Likewise the amplifier JFET data sheet for the 2N4867 series offers parameters not found on the switching JFET data sheet.

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NCB
See Section 4

BENEFITS

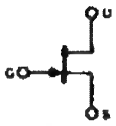
- Low Insertion Loss, High Accuracy in Test Systems $r_{DS(on)} < 30\ \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

2N4391 2N4392 2N4393 PREFERRED PARTS FN4392 SERIES, PLASTIC EQUIVALENT
PN4391 SERIES SURFACE MOUNT EQUIVALENT: SST111 SERIES/SST4391 SERIES

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 6



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	2N4391 Min	2N4391 Max	2N4392 Min	2N4392 Max	2N4393 Min	2N4393 Max	Unit	Test Conditions		
1	STATIC	I_{GSS} Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0		
2				200		-200		-200	nA			150°C
3		BV_{GSS} Gate Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$I_{D(off)}$ Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = -5 V	
5								200	nA			150°C
6						100			pA		V_{GS} = -7 V	
7						200			nA			150°C
8				100					pA		V_{GS} = -12 V	
9				200					nA			150°C
10		$V_{GS(f)}$ Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
11		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-6	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA		
12		I_{DSS} Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
13		$V_{DS(on)}$ Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
14						0.4					I_D = 6 mA	
15				0.4							I_D = 12 mA	
16		$r_{DS(on)}$ Static Drain Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
17		$r_{ds(on)}$ Drain Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
18	DYN	C_{iss} Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
19		C_{rss} Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = -8 V	
20						3.5					V_{GS} = -7 V	
21				3.5							V_{GS} = -12 V	
22	SW	$t_{d(on)}$ Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
23		t_r Rise Time		5		5		5				
24		$t_{d(off)}$ Turn-OFF Delay Time		20		35		50				
25		t_f Fall Time		15		20		30				

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4391	12 mA	-12 V	
2N4392	6	-7	
2N4393	3	-5	

*JEDEC registered data

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%

NCB

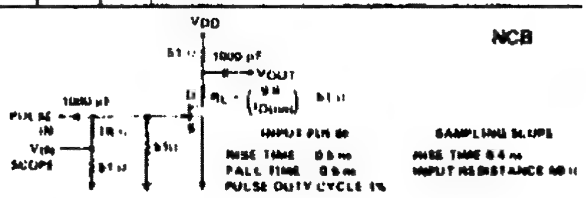


Figure 7.1 2N4391-3 Switching JFET data sheet. (Reprinted with permission of Siliconix inc.)

n-channel JFETs designed for . . .

Siliconix

Performance Curves NPA
See Section 4

■ Audio and Sub-Audio Amplifiers

BENEFITS

- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/$\sqrt{Hz}$ Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/$\sqrt{Hz}$ Typical at 1 kHz

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Souce Voltage (Note 1) ... -40 V
Gate Current or Drain Current ..... 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C) .....300 mW
Storage Temperature Range ..... -65°C to +200°C
Lead Temperature
(1/16" from case for 60 seconds) .....300°C

TO-72
See Section 6

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

			Characteristic	2N4867 2N4867A Min	2N4867 2N4867A Max	2N4868 2N4868A Min	2N4868 2N4868A Max	2N4869 2N4869A Min	2N4869 2N4869A Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0		
2					-0.25		-0.25		-0.25	μA			150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-6		V_{DS} = 20 V, I_D = 1 μA		
5		I_{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	μmho	V_{DS} = 20 V, V_{GS} = 0		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5		4		10				
8		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF			f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		25		25		25				
10		$\overline{e_n}$	Short Circuit Equivalent Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	2N4867 Series	f = 10 Hz
11					10		10		10			2N4867A Series	
12					10		10		10			2N4867 Series	f = 1 kHz
13					5		5		5			2N4867A Series	
14		NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0 R_{gen} = 20 K, 2N4867 Series 5 K, 2N4867A Series		f = 1 kHz

*JEDEC registered data

NPA

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms

Figure 7.2 2N4867-9 Amplifier JFET data sheet. (Reprinted with permission of Siliconix inc.)

2N5564 2N5565 2N5566
PREFERRED PARTS DN5564 SERIES

matched dual n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NCB
See Section 4

- **Wideband Differential Amplifiers**
- **Commutators**

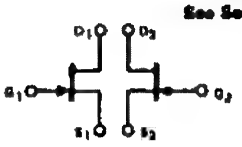
BENEFITS

- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, T_A = 25°C (Derate 3.3 mW/°C)	660 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-71
See Section 8



Bottom View

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS} Gate-Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2				-200	nA		150°C
3		BV_{GSS} Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$ Gate Source Cutoff Voltage	-0.5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$ Gate Source Voltage		1.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS} Saturation Drain Current (Note 1)	5	30	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$ Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs} Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
			7000				f = 100 MHz
9		g_{os} Common-Source Output Conductance		45			f = 1 kHz
10		C_{rss} Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss} Common-Source Input Capacitance		12			
12		NF Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		e_n Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristic	2N5564 Min	2N5564 Max	2N5565 Min	2N5565 Max	2N5566 Min	2N5566 Max	Unit	Test Conditions	
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$ Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$ Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$ Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C, T_B = 125°C
				10		25		50			T_A = -55°C, T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$ Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

*JEDEC registered data.

NCB

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%
2. Assumes smaller value in numerator
3. Measured at ends points, T_A and T_B

Figure 7.3 2N5564-66 Dual JFET data sheet. (Reprinted with permission of Siliconix inc.)

Comparing Figures 7.1 and 7.2, we find:

Switching JFET	Amplifier JFET
$r_{DS(on)}$	g_{fs}
$V_{DS(on)}$	g_{os}
$I_{D(off)}$	NF
$t_{d(on)}$	$\bar{e}_n$
t_r	
$t_{d(off)}$	
t_f	

All these symbols have been fully covered in Chapter 3.

If the headline of the data sheet does not clearly identify application, surely the symbols leave no doubt. The differential-pair JFET (Figure 7.3) is equally obvious; it may provide several differential parameters, such as:

$$I_{DSS1}/I_{DSS2} \quad \text{and} \quad g_{fs1}/g_{fs2}$$

as well as differential gate-source voltages both with and without temperature-drift characteristics:

$$\frac{|V_{GS1} - V_{GS2}|}{\Delta T} \quad \text{and} \quad |V_{GS1} - V_{GS2}|$$

There are hundreds of JFET data sheets, but there are not hundreds of JFETs. Quite likely there may be only a few dozen silicon JFET geometries worldwide! The proliferation of data sheets (and part numbers) principally results from the distribution of $V_{GS(off)}$ and with it, the parameters that are intimately related: $r_{DS(on)}$, I_{DSS}, and g_{fs} (see Eqs. 5.5–5.11). As we review the typical JFET data sheet, we are apt to see several consecutive part numbers differing only in these four parameters (not addressing the differential-pair device).

We know that in fabricating a JFET, the deeper the gate diffusion, the lower the magnitude of gate-source cutoff voltage

$|V_{GS(off)}|$. We also know that several of the fundamental parameters are directly (and mathematically) related to $V_{GS(off)}$. Since wafer fabrication is not an exact science (despite hushed protestations to the contrary), we must anticipate that every wafer run will result in a statistical distribution of electrical parameters. In other words, we will witness a distribution of $V_{GS(off)}$ and with it, a distribution of such major parameters as I_{DSS}, $r_{DS(on)}$, and g_{fs}. Additionally, because mask misalignments may occur, as well as other anomalies of manufacture, we may also discover this distribution to be skewed in unpredictable ways.

As we review and compare JFET data sheets, we may discover that $V_{GS(off)}$ for some is established for an I_D of 1 nA, whereas others are at differing drain currents, for example, at 0.1 μA. Fortunately we can reconcile these differences. A rule of thumb says that for every decade change in I_D we change $V_{GS(off)}$ by 0.1 V. However, there are restrictions; this rule of thumb does not extend much above 1 μA.

We know that $V_{GS(off)}$ is perhaps the single most important JFET parameter, for as it varies so do most of the critical parameters: I_{DSS}, $r_{DS(on)}$, and g_{fs} are intimately related to $V_{GS(off)}$ as well as to each other. To illustrate, let us take the critical parameters of the 2N4392 offered on the data sheet:

	Min	Max	Unit
$V_{GS(off)}$	−2	−5	V
I_{DSS}	25	75	mA
$r_{DS(on)}$		60	Ω

Can we ever expect to find a 2N4392 with an ON resistance under 10 Ω? The data sheet does not specify a minimum value. But it is likely? We shall soon see that it is not. If we want a JFET with the same $V_{GS(off)}$ and I_{DSS} but with substantially lower $r_{DS(on)}$, we need to look to a different data sheet. (*Hint*: Try a larger geometry, such as the 2N5434.)

In Chapter 5 we examined how parameters interact. The graphical representation in Figure 5.9, showing the relationship between $V_{GS(off)}$, $r_{DS(on)}$, and I_{DSS} of the 2N4391 series is extremely helpful in understanding the data sheet. If we compare the switching JFET data sheet (Figure 7.1) with the graphical relationship of the parameters, repeated with added emphasis

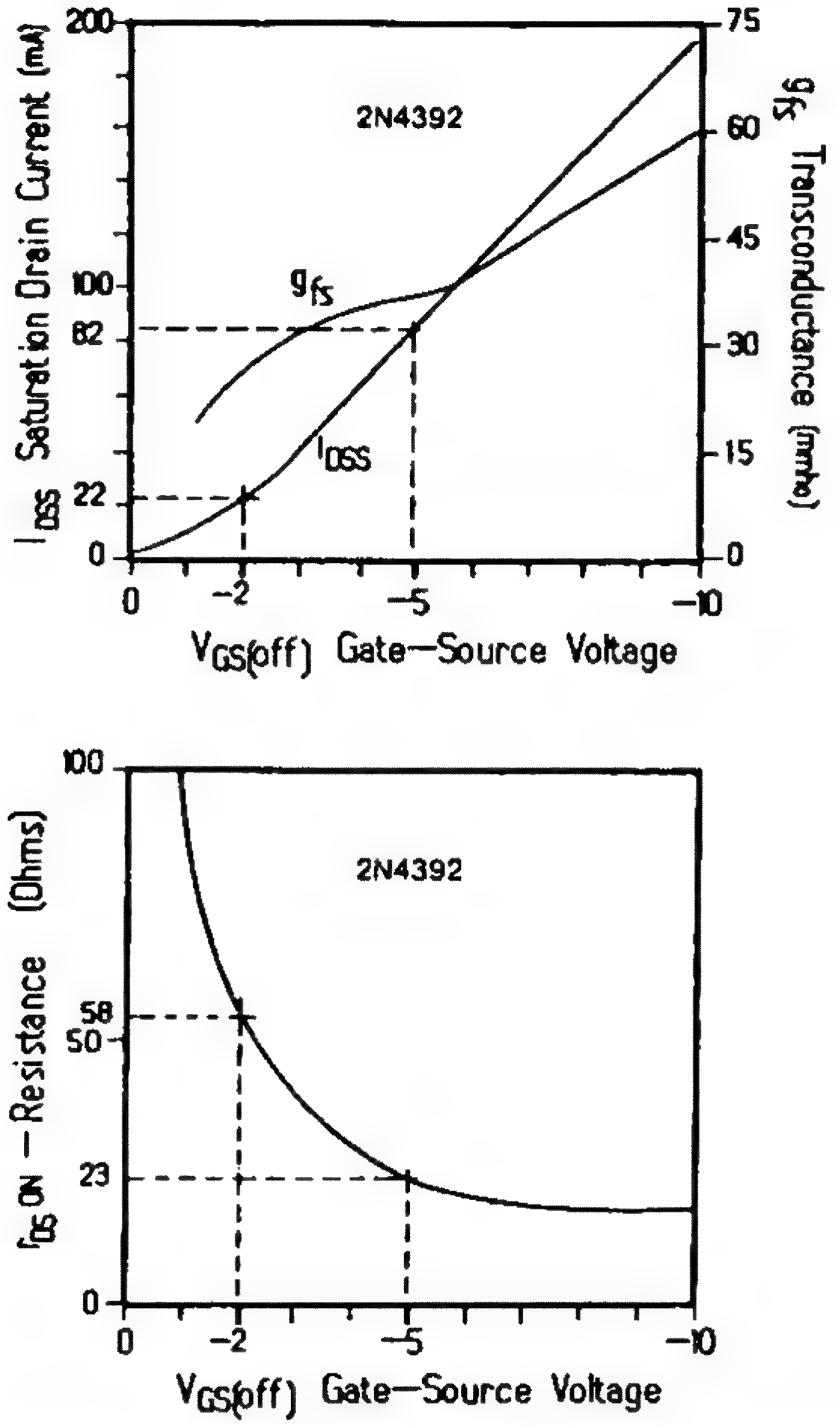


Figure 7.4 General parameter relationships for the 2N4391-series JFET, emphasizing the parameter limits for the 2N4392. Note how the data sheet limits compare with the limits determined by these curves. (Reprinted with permission of Siliconix inc.)

in Figure 7.4, it becomes clear how the three switching JFETs' characteristics are derived. As the magnitude of $V_{GS(off)}$ rises, by virtue of the statistical distribution resulting from the diffusion process, we see both I_{DSS} and g_{fs} rise and $r_{DS(on)}$, drop, as we would expect.

Table 7.1 Matrix for 2N4391 Series

Series	$V_{GS(off)}$ min	I_{DSS} min	$r_{DS(on)}$ max
2N4391	−4 V	61 mA	31 Ω
2N4392	−2 V	22 mA	58 Ω
2N4393	−0.5 V	8 mA	100 Ω
	$V_{GS(off)}$ max	I_{DSS} max	$R_{DS(on)}$ min
2N4391	−10 V	190 mA	15 Ω
2N4392	−5 V	82 mA	23 Ω
2N4393	−3 V	41 mA	40 Ω

Relying on the parameter $V_{GS(off)}$ and the distribution offered in Figure 7.4, we can develop the matrix presented in Table 7.1.

Comparing the data in Table 7.1 with the characteristics offered on the data sheet, we find excellent correlation. Of special interest, the matrix offers insight into nonregistered parameters, such as the minimum value of $r_{DS(on)}$, which is missing from Figure 7.1. Some data sheets offer far less information (Figure 7.5), but we can use this technique to construct a more detailed matrix. However, remember that only the data sheet establishes your *guaranteed* specifications. The added benefit is that the matrix may show your JFET to have a tighter distribution than was identified by the data sheet parameters.

Ignoring the thermal ratings, as we read in Chapter 6, may be dangerous. For some JFETs we have no problem, but for some large-geometry devices, such as this example (the 2N4391 series), even if I_{DSS} times V_{DS} is less than the 1.8 W specified on the data sheet, we must not overlook that the data sheet states "@ 25°C case temperature." In the unlikely event that a 2N4392 is operating at I_{DSS} and at a V_{DS} of 20 V, 1.5 W will generate considerable heat.

Device dissipation, as provided on the data sheet, may appear to have little rationale. Most JFET semiconductor die are quite small, running from as small as 0.16 mm^2 up to 1.35 mm^2. As a consequence, the package and its mounting dictate the power-handling capability of the JFET.

SURFACE MOUNT EQUIVALENT: SST111, SST112, SST113

J111 J112 J113

n-channel FETs designed for . . .

- Analog Switches
- Choppers
- Commutators

Siliconix

Performance Curves NCB See Section 4

BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $r_{DS(on)} < 30\ \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{d(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

Plastic

TO-92
See Section 8

Bottom View

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –35V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic	J111 Min	J111 Typ	J111 Max	J112 Min	J112 Typ	J112 Max	J113 Min	J113 Typ	J113 Max	UNIT	Test Conditions
1	STATIC	I_{GSS} Gate Reverse Current (Note 1)			1			1			1	nA	V_{DS} = 0 V, V_{GS} = 15 V
2		$V_{GS(off)}$ Gate Source Cutoff Voltage	3		10	1		5			3	V	V_{DS} = 5 V, I_D = 1 µA
3		BV_{GSS} Gate Source Breakdown Voltage	35			35			35				V_{DS} = 0 V, I_G = 1 µA
4		I_{DSS} Drain Saturation Current (Note 2)	20			5			2			mA	V_{DS} = 15 V, V_{GS} = 0 V
5		$I_{D(off)}$ Drain Cutoff Current (Note 1)			1			1			1	nA	V_{DS} = 5 V, V_{GS} = 10 V
6		$r_{DS(on)}$ Drain Source ON Resistance			30			50			100	Ω	V_{DS} = 0.1 V, V_{GS} = 0 V
7	DYNAMIC	$C_{d(off)}$ Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0 V, V_{GS} = 10 V; f = 1 MHz
8		$C_{s(off)}$ Source Gate OFF Capacitance			5			5			5		
9		$C_{d(on)}$ + $C_{s(on)}$ Drain Gate Plus Source Gate ON Capacitance			28			28			28		V_{DS} = V_{GS} = 0; f = 1 MHz
10		$t_{d(on)}$ Turn ON Delay Time		7			7			7		ns	Switching Time Test Conditions: J111 / J112 / J113
11		t_r Rise Time		6			6			6			V_{DD}: 10 V / 10 V / 10 V
12		$t_{d(off)}$ Turn OFF Delay Time		20			20			20			$V_{GS(off)}$: -12 V / -7 V / -5 V
13		t_f Fall Time		15			15			15			R_L: 800 Ω / 1,600 Ω / 3,200 Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 µs; duty cycle ≤ 3%.

NCB

Figure 7.5 J111-113 switching JFET data sheet. (Reprinted with permission of Siliconix inc.)

Another area of some confusion is the operating temperature range, often conveniently omitted from the data sheet. The storage temperature range is easier to find. Regardless of whether the maximum operating temperature is provided, the power derating specifications are, and using the derating we can derive a maximum operating temperature, T_{max}, if necessary:

$$t_{max} = \frac{\text{total device dissipation}}{\text{(linear) power derating}} + 25°C \ (°C) \qquad (7.1)$$

Some dual JFETs (Figure 7.3) will provide *two* power ratings and two deratings, one labeled "each side," the other, "both sides." If you are using both sides, be sure you use the "both sides" deratings in Eq. 7.1; otherwise you may exceed the maximum permissible operating temperature of the die. Generally the "both sides" power rating is twice the "each side" rating, but the derating factor is not, because of thermal interactions within the header.

Should your end use for this switching JFET be for a sample and hold circuit, be advised that the 2N4392 is a very poor choice! Note that C_{rss} is specified beyond gate-source cutoff, and for a good reason. For switching-type JFETs, such as we have in Figure 7.1, C_{rss} is measured at a gate voltage at or beyond cutoff. Gate-drain capacitance (C_{rss}) of a switching-type JFET affects it charge-transfer characteristics. The effect becomes especially critical in sample and hold applications, shown in Figure 7.6. When the JFET switch is OFF (as shown in the equivalent circuit), C_{gd} (C_{rss}) forms a capacitive voltage divider with $C_{storage}$, resulting in the coupling of charge into $C_{storage}$. The error introduced can be approximated by:

$$d_V = \frac{dQ}{C_{storage}} \qquad (7.2)$$

For JFETs used as amplifiers, C_{rss} is usually offered at full operational ratings, as are the other capacitance specifications.

Most JFET data sheets that have been characterized for amplifier service (Figures 7.2 and 7.3) include a noise specification, identified as either $\bar{e}_n$ (noise voltage) or NF (noise figure) at some reasonably low audio frequency. The former given as a ratio: nanovolts per square root of hertz ($nV/Hz^{1/2}$), the latter in decibels (dB).

To ensure selecting the right JFET for the job, we must understand how to interpret noise specifications. Noise figure

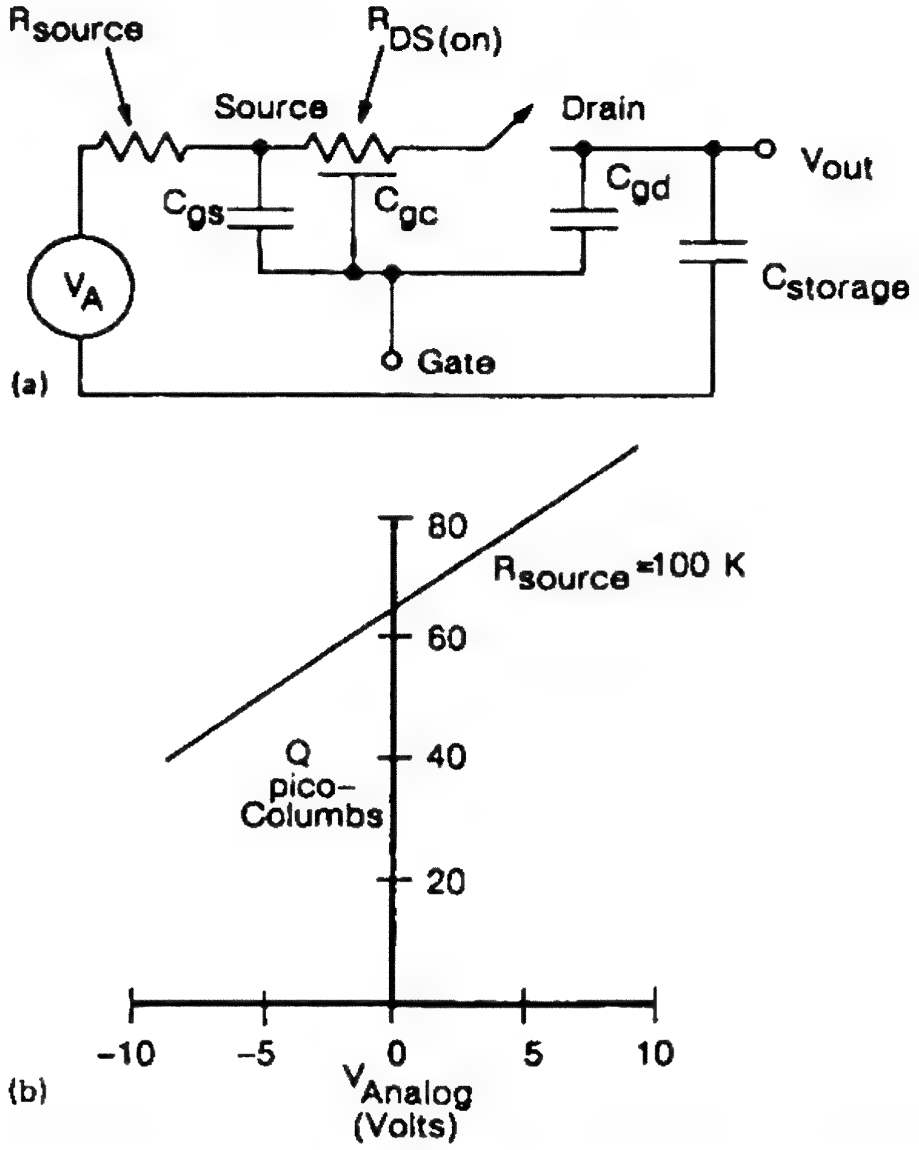


Figure 7.6 (a) Equivalent circuit of a sample and hold circuit, showing the parasitic capacitances that contribute to charge-coupled errors. (b) Typical charge-coupling error expressed in picocoulombs for a 2N4392 JFET switch with a source resistance of 100 kΩ.

must be accompanied with reference to a specific generator resistance, as was earlier defined by Eq. 3.13. To illustrate, let us select the lowest noise JFET from the following two specifications:

$$\text{NF} = 0.5 \text{ dB} \quad \text{at} \quad R_G = 1 \text{ M}\Omega$$

$$\text{NF} = 3.0 \text{ dB} \quad \text{at} \quad R_G = 1 \text{ k}\Omega$$

all other parameters (temperature and bandwidth) being equal. Using Figure 3.7 we discover that the JFET sporting a 3 dB

noise figure has only 4 $nV/Hz^{1/2}$ of noise ($\bar{e}_n$) compared to 44 $nV/Hz^{1/2}$ for the 0.5 dB JFET. What has made the difference is the *generator impedance*.

A noise phenomenon that also needs attention is the effect of (low) flicker noise, or 1/f noise. In Figure 3.6 we saw that at frequencies below 200-500 Hz, the noise voltage rises dramatically. Some data sheets identify this 1/f noise by offering $\bar{e}_n$ at 10 Hz, whereas others mask the effect by providing $\bar{e}_n$ (or NF) at higher test frequencies, such as at 1 kHz or above, out of the region of 1/f flicker noise and well into the Johnson noise region.

How do we compare JFETs when one offers $\bar{e}_n$ at 10 Hz and another at 1 kHz? Unless the vendor has provided supporting data elsewhere in the catalog, we can't unless we measure $\bar{e}_n$ for each device.

The amplifier-type JFET data sheet provided in Figure 7.2 (2N4867-series) provides *both* $\bar{e}_n$ and NF. The latter, according to Eq. 3.14, not only reaffirms $\bar{e}_n$ but also ensures that the noise *current* $\bar{i}_n$ is low, as well.

Within the family of JFETs we find some characterized for high-frequency (to about 500 MHz) amplifier service. For these, noise figure has a different meaning because it does not represent a noise *voltage*, but a noise *current* (shot noise) phenomenon. We seldom find the generator impedance for these high-frequency JFETs on the data sheet, and to assume 50 Ω would be presumptuous.

Operating gate current, I_G, regrettably not found on many JFET data sheets, offers a critical inside look into the performance of the JFET. First, it warns us of the maximum V_{DG} and I_D to maintain a high gate-input impedance (see Eq. 3.2); second, it identifies how we may keep the noise current low (see Eq. 3.14).

Dual JFETs have unique problems. There are two types of dual: monolithic and two-chip. The advertized advantage of the dual is that both sides supposedly drift together. That may be true for the monolithic dual, but for the two-chip dual we need to be on guard.

All JFETs exhibit a zero TC (zero temperature coefficient), and to improve the drift characteristics of the dual, the drain current is generally specified at or near this zero TC value. An estimate of the gate-source voltage required for an n-channel JFET to achieve zero TC is:

$$V_{GSZ} \approx V_{GS(off)} + 0.7\ V \qquad (7.3)$$

Data sheets are quite consistent in defining the temperatures used to qualify the drift specifications of duals. Three temperatures are specified, at:

−25, +25, and +125°C

They are grouped to show two drift tests covering the following ranges:

Test 1 +25 to +125°C
Test 2 −55 to +25°C

Despite their consistency in defining the temperature differentials, the specifications are anything but consistent otherwise. Scrutiny of the dual JFET data sheet indicates that test 1 covers a range of 100°C, whereas test 2 spans a range of only 80°C. Yet, the electrical specifications are *always* identical!

It should not be surprising that the thermal characteristics of a monolithic dual are superior to that of a two-chip dual. Since the drift characteristics offered on the data sheet are guaranteed *only for the three test temperatures*, we would be better served in using monolithic duals—especially if our application requires close drift specifications at temperatures other than those offered on the data sheet.

Yet, the monolithic dual is not a panacea in every application. Most duals are junction isolated, and since the pn junctions may form parasitic bipolar transistors, latch-up could occur if we were to use the monolithic dual in a cascade arrangement. Careful analysis of the pn junctions reveals a vertical npn and a lateral pnp (as shown in Figure 7.7), which together may form an SCR if the multiple of betas ($\beta_{npn} \times \beta_{pnp}$) is 1 or more. There are times when a two-chip dual is preferred, despite its inherent drift problem.

7.2.2 Scrutinizing the Small-Signal MOSFET Data Sheet

Don't ignore this warning: *MOSFETs are static sensitive.* The most important static-sensitive element is the gate. It matters little what its BV_{GSS} rating may be, the MOSFET can be destroyed by mishandling. If you feel or hear the static, you have already far exceeded the electrostatic voltages necessary to destroy the MOSFET. Don't rely on zener-protected gates;

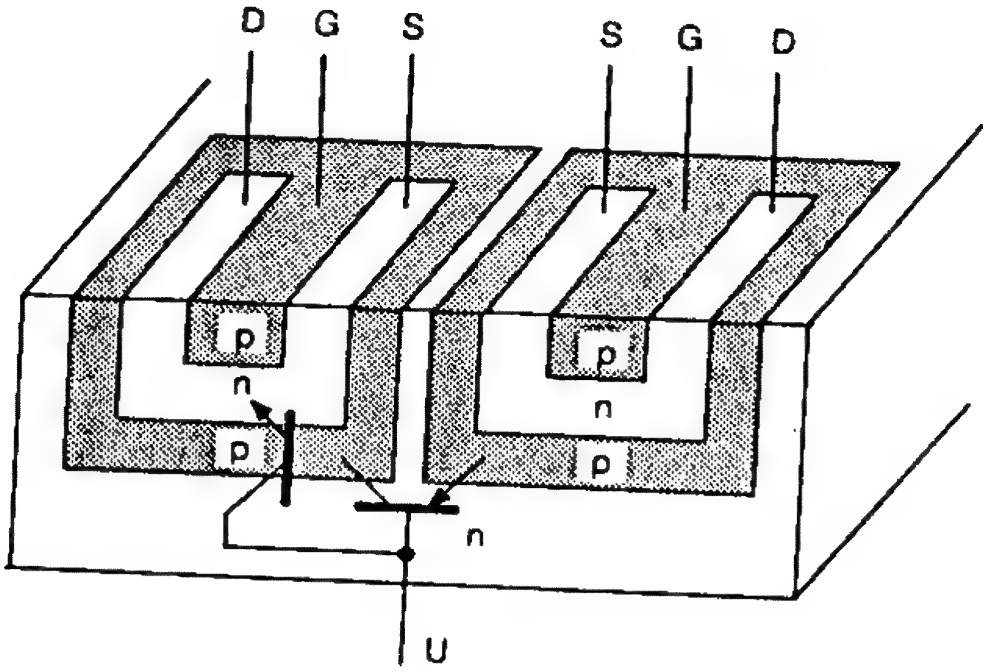


Figure 7.7 Parasitic npn and pnp transistors, characteristic of junction-isolated monolithic dual JFETs, may form an SCR (latch-up) effect if substrate is left floating and one gate is biased higher than the opposing source.

handle all MOSFETs with caution. Remember that although silicon dioxide can withstand approximately 6×10^6 V/cm, this common gate-oxide barrier may be only 80 nm (80×10^{-11} cm) thick.

Take special precautions in handling because destructive electrostatic voltages are everywhere. Antistatic materials generally exhibit surface resistivities ranging from $>10^{18}$ to $>10^{14}$ Ω/square. The less water-absorptive the material, the greater its likelihood of generating destructive electrostatic potentials. The hygroscopic materials best suited for antistatic packaging include virgin cotton, cellulose-based hardboards, wood and paper products, and some melamine laminates. The Tirboelectric chart has little meaning in determining potentially destructive electrostatic charges because *any* charge can be destructive.

Unlike the depletion-mode JFET, the MOSFET exists in eithe of two modes, enhancement or depletion, as well as, of course, as either n-channel or p-channel.

On the surface, having so many potential options, we might erroneously conclude that there are, indeed, many available options. Regrettably, not so. We find few vendors of small-signal MOSFETs and they offer few options.

In the unlikely event that the headline on the data sheet fails to identify the mode of operation, differentiating between the enhancement and depletion modes is easily accomplished during a cursory examination of the data sheet.

If the data sheet is defining an enhancement-mode MOSFET, we will, in all likelihood, find the symbol for threshold voltage, $V_{GS(th)}$ or V_T. Additionally, we may find I_{DSS} or $I_{D(off)}$ or $I_{DS(off)}$ (with the test conditions of $V_{GS} \leq 0$ V) identified as drain *cutoff* current, or leakage current; and, last, possibly the symbol $I_{D(on)}$ (with the test conditions of $V_{GS} \neq 0$). If such a poorly edited data sheet is describing a depletion-mode MOSFET, then, rather than finding the symbol for threshold voltage, we should find, as we did for the JFET, $V_{GS(off)}$—gate-source cutoff voltage. Added to this, we may find I_{DSS} defined as we would expect for a depletion-mode FET. The symbol $I_{D(off)}$, if present, would *not* have the same meaning as I_{DSS}, as was the case for the enhancement-mode MOSFET.

Unlike the JFET, neither $V_{GS(off)}$ nor $V_{GS(th)}$ is intimately related to the other major parameters. Both $V_{GS(off)}$ and $V_{GS(th)}$ are lot sensitive, (because of their sensitivity to the oxide thickness), not scatter sensitive.

The small-signal MOSFET, unlike the JFET, is basically a four-terminal structure consisting of a source, drain, gate, *and* substrate. The substrate may be internally bridged to the source for some MOSFETs. But if not—if the substrate exits to a separate pin—then $V_{GS(th)}$ (for the enhancement-mode MOSFET) or $V_{GS(off)}$ (for the depletion-mode MOSFET) may be affected by the substrate bias. Take careful note of the test conditions pertaining to the gate bias and note the condition of V_{BS} (or V_{SB})—body-source substrate voltage. As the magnitude of the substrate voltage rises (positively for a p-channel MOSFET, negatively for an n-channel MOSFET), the magnitude of the threshold voltage may also rise (negatively for a p-channel and positively for an n-channel MOSFET), and sometimes quite dramatically, as shown in Figure 7.8.

Capacitance of a MOSFET may be envisioned, as we did in Figure 1.7, as parallel plates separated by a dielectric medium. However, unlike the JFET, the gate-to-source capacitance C_{gs}, as well as the gate-to-drain capacitance C_{gd}, of the small-signal, enhancement-mode MOSFET may undergo a dramatic increase when channel conduction occurs, as shown in Figure 7.9.

An enhancement-mode MOSFET, being normally OFF when no bias is applied, may appear to offer superior performance as an analog switch. Watch out, and remember that when the analog

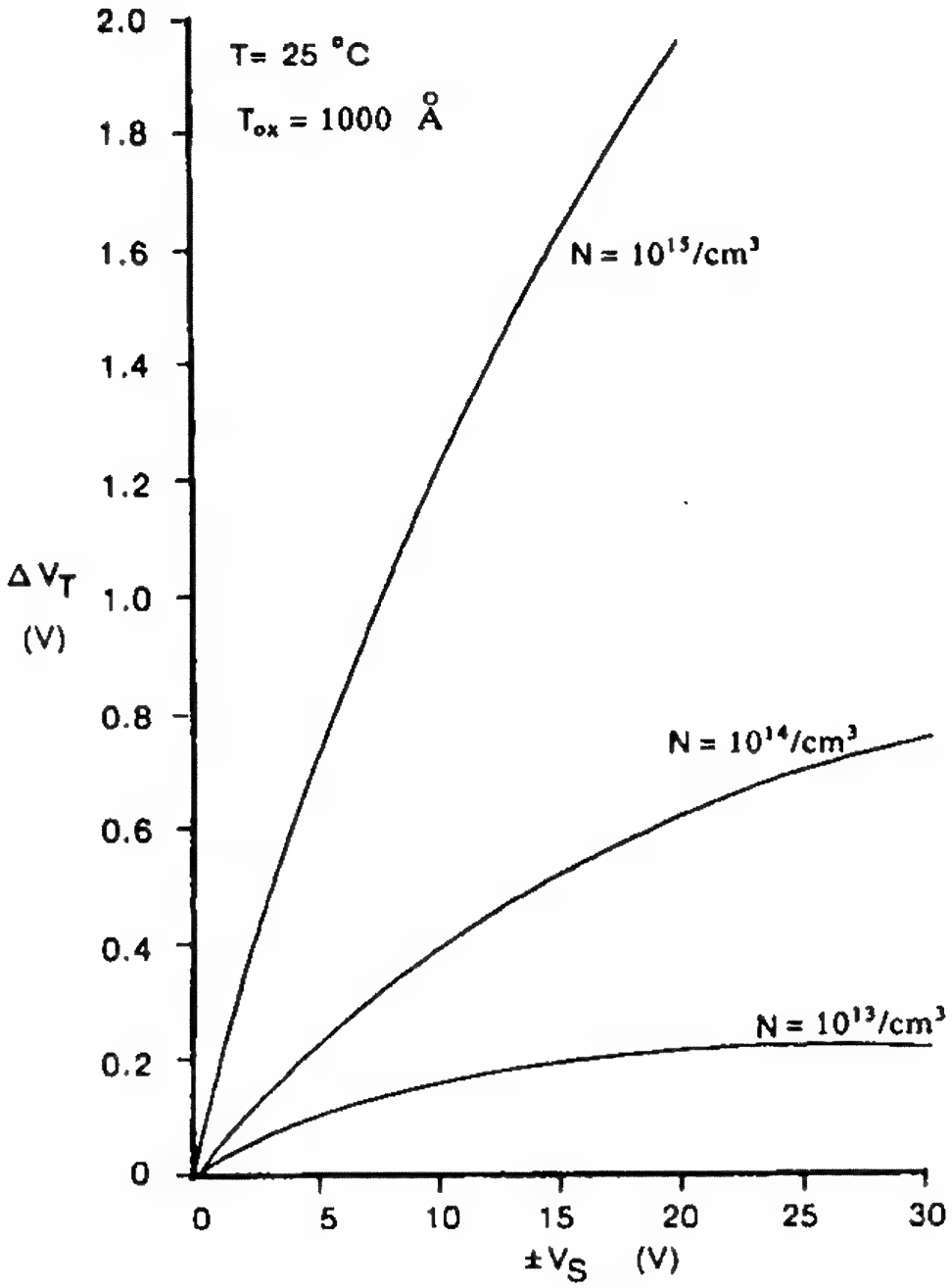
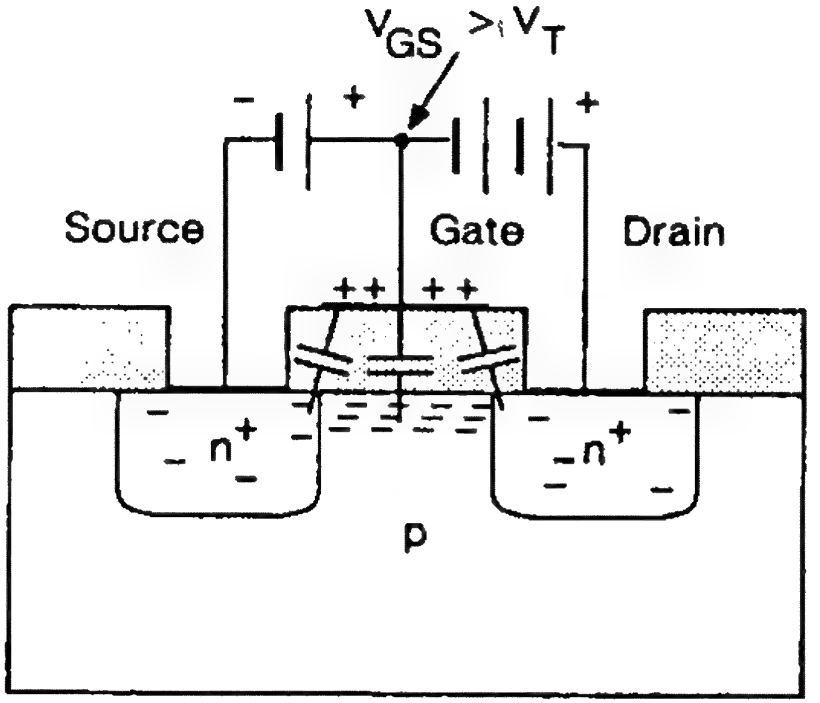


Figure 7.8 Variation of threshold voltage with applied substrate-to-source bias per 1000 nm of silicon dioxide gate insulator for n- and p-channel MOSFETs at 25°C, as a function of doping concentrations. (From Richman, *MOS Field-Effect Transistors and Integrated Circuits*. Copyright © 1973 John Wiley & Sons, Inc. Reprinted by permission of John Wiley & Sons, Inc.)

voltage (riding on the source) approaches the gate bias V_{GG}, V_{GS} drops, resulting in a rapid rise in $r_{DS(on)}$. The net result is called *resistance modulation* distortion, as defined by the following equations:



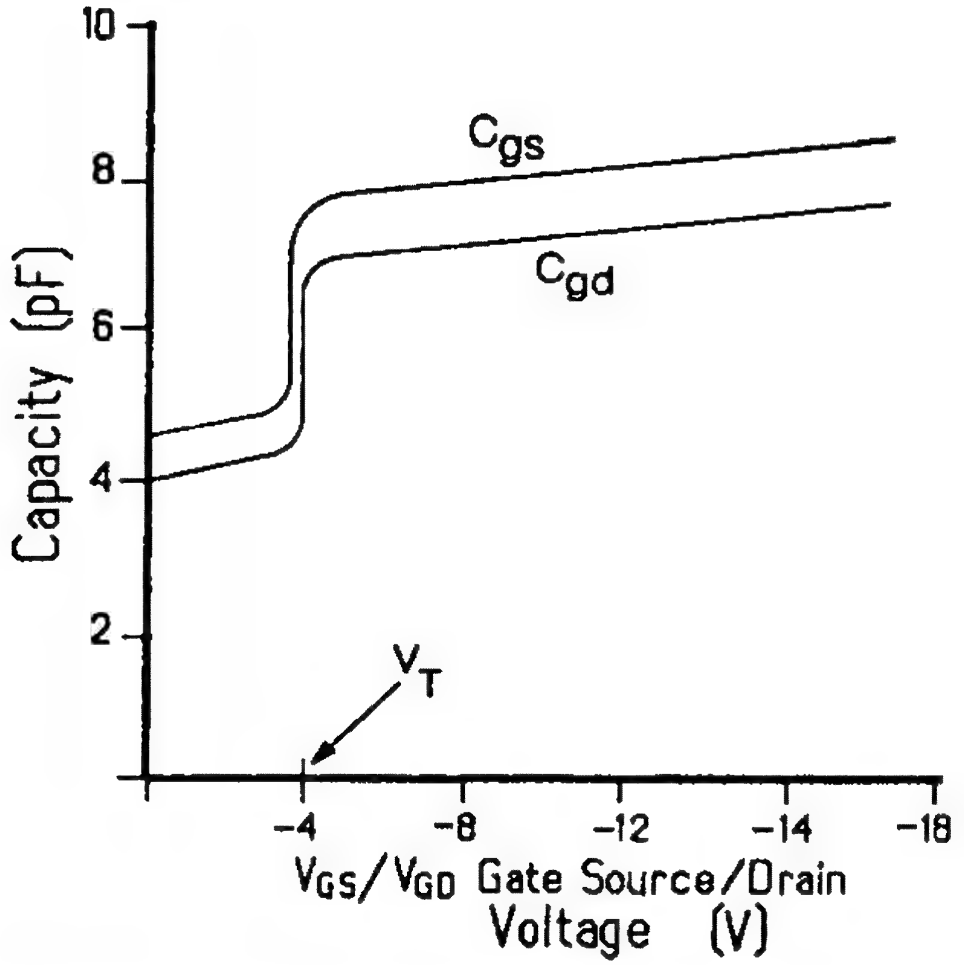


Figure 7.9 Effect of channel conduction of an n-channel enhancement-mode MOSFET on capacitance. At threshold, channel conductance commences and capacitance takes a dramatic upward leap.

$$V_{out} = \frac{R_L}{r_{DS(on)} + R_L + R_G} V_A \tag{7.4}$$

$$\% \text{ distortion} = \frac{dr_{DS(on)}}{R_G + R_L + r_{DS(on)} + dr_{DS(on)}} \tag{7.5}$$

where

$dr_{DS(on)}$ = *change* in ON resistance with bias
V_A = analog signal voltage
R_L = load resistance
R_G = generator, or source, resistance

Seldom do we find the noise voltage on a MOSFET data sheet. A small-signal MOSFET may exhibit a noise voltage 10 to 20 times that of a JFET. Unfortunately, there are no MOSFETs with a low value of $\bar{e}_n$ to match that of a JFET.

7.2.3 Scrutinizing the SIT Data Sheet

At the time of writing the static-induction transistor had yet to find a market. Consequently, there were few data sheets available. One data sheet that clearly illustrates the considerable power capability of the SIT is offered in Figure 7.10, where a total power dissipation of 3000 W is claimed!

Because of the uniquely low RC time constant inherent with the SIT, this transistor may lend itself to very-high-frequency applications.

Quite possibly the most notable parameter is the gate-source cutoff voltage $V_{GS(off)}$ that identifies the SIT as a depletion-mode FET, and, in addition, indicates a surprisingly high cutoff voltage when compared with most power FETs.

Because the SIT exhibits a triodelike output characteristic (see Figure 2.7), we should expect to find a parameter identifying the voltage gain μ, as indeed we do (Eq. 4.11). Because of its high output conductance g_{os}, the voltage gain μ (or A_v), is, at best, moderate.

A rule of thumb offers us guidance to determine the magnitude of $V_{GS(off)}$ if it is not provided on the data sheet:

$$|V_{GS(off)}| \cong \frac{1.25\ V_{(BR)DSX}}{\mu} \tag{7.6}$$

ABSOLUTE MAXIMUM RATINGS (T_A=25 C)			
Term	Symbol	Condition	Limits
Storage Temperature	T_{stg}		-50° +150 °C
Operating Junction Temperature	T_j		+150 °C
Gate to Source Voltage	V_{GSO}		70 V
Gate to Drain Voltage	V_{GDO}		1500 V
Gate Current	I_G	V_{GS}=1 V	0.5 A
Drain Current	I_D		180 A
Total Power Dissipation	P_T		3000 W
ELECTRICAL CHARACTERISTICS (T_A=25 C)			
Gate to Source Breakdown Voltage	$V_{(BR)GSO}$	I_G= 0.2 mA	70 V
Gate Leakage Current	I_{GSS}	V_{GS} = -40 V	200 μA
Drain Cut-Off Current	$I_{D(off)}$	V_{GS} = -50 V	200 μA
Drain Currrent	I_{DSS}	V_{GS}= 0 V_{DS}= 10 V	25 A
Gate to Source Cut-Off Voltage	$V_{GS(off)}$	V_{DS}= 300 V I_D = 1 mA	20 V
Gate to Drain Breakdown Voltage	$V_{(BR)GDO}$	I_D= 0.2 mA	1500 V
Insertion Gain	μ	V_{GS}= -20 V I_{DS}= 0.1 A	12
Input Capacity	C_{iss}	V = 10 V f = 250 kHz	25000 pF
Cut-Off Frequency	f_T	V = 20 V I_D= 2 A	7 MHz
Drain to Source ON Resistance	r_{ON}	V_{GS}= 0 I_D= 2 A	0.5 Ω
Drain to Source OFF Resistance	r_{OFF}	V_{DS}= 300 V V_{GS}= -50 V	1 MΩ min.
Turn-ON Time	t_{on}	I_D = 1.5 A V_{DS}= 50 V	350 ns
Turn-OFF Time	t_{off}		350 ns

Figure 7.10 2SK182-183 Static-induction transistor data sheet. (Reprinted with permission of Tokin, Ltd.)

The data sheet shown in Figure 7.10 lends some confusion in its characterization of input capacitance (C_{iss}) by its imprecise reference to V_{DS}, *not* to V_{GS}, as we might have anticipated. Since this capacitance, like all FET capacitances, is depletion-field dependent, as V_{DS} rises, the capacitance will decrease.

7.2.4 Scrutinizing the Power DMOSFET Data Sheet

During the formative years when power DMOSFET technologists were more interested in proliferating part numbers than in production, every vendor seemed to offer a novel format, as well as a more novel identifying part number. Possibly because of pressure to acquire military-qualified parts, in the early to mid-1980s JEDEC registration bacame popular for power DMOSFETs. With JEDEC registration followed by MIL-STD-750C qualification (see Appendix B to Chapter 3), we are now finding one data sheet format taking precedence.

When we read data sheets, we tend to accept certain specifications without question, even if we know that in combination they are incompatible. For example, we find a power DMOSFET with an operating voltage of 400 V and a continuous drain current rating of 15 A, for a total of 6000 W! Yet, that particular power DMOSFET (an IRF350) is rated at only 150 W. This sort of inconsistency is accepted without question for any transistor. We accept the obvious fact that we cannot operate at both limits simultaneously.

But there are other hidden inconsistencies within the data sheet that, perhaps, might not be so well accepted. For our example, let us continue with the IRF350, shown in Figure 7.11. Several of the vendors offering this part provide a product summary in the headline of the data sheet. Within this headline we generally find the following,

Part number	$V_{(BR)DSS}$ volts	$r_{DS(on)}$ (Ohms)	I_D (Amps)
IRF350	400	0.3	15

In the column identified as the absolute maximum ratings, we find:

I_D @ T_C = 25°C 15 A

Siliconix incorporated

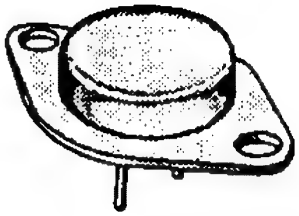
IRF350, IRF351 IRF352, IRF353

N-Channel Enhancement Mode Transistors

MOSPOWER

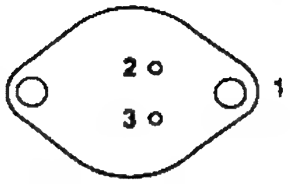
PRODUCT SUMMARY

PART NUMBER	$V_{(BR)DSS}$ (VOLTS)	$r_{DS(on)}$ (OHMS)	I_D (AMPS)
IRF350	400	0.3	15
IRF351	350	0.3	15
IRF352	400	0.4	13
IRF353	350	0.4	13



TO-204AA (TO-3)

BOTTOM VIEW



1 DRAIN (CASE)
2 GATE
3 SOURCE

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	IRF 350	IRF 351	IRF 352	IRF 353	Units
Drain-Source Voltage		V_{DS}	400	350	400	350	V
Gate-Source Voltage		V_{GS}	± 40	± 40	± 40	±40	
Continuous Drain Current	T_C = 25°C	I_D	15	15	13	13	A
	T_C = 100°C		9.0	9.0	8.0	8.0	
Pulsed Drain Current[1]		I_{DM}	60	60	52	52	
Avalanche Current		I_A	15	15	15	15	
Power Dissipation	T_C = 25°C	P_D	150	150	150	150	W
	T_C = 100°C		60	60	60	60	
Operating Junction & Storage Temperature Range		T_J, T_{stg}	-55 to 150				°C
Lead Temperature (1/16" from case for 10 secs.)		T_L	300				

THERMAL RESISTANCE RATINGS

THERMAL RESISTANCE	Symbol	Typ.	Max.	Units
Junction-to-Case	R_{thJC}	-	0.83	K/W
Junction-to-Ambient	R_{thJA}	-	30	
Case-to-Sink	R_{thCS}	0.1	-	

[1]Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)

Figure 7.11 IRF350-353 Power DMOSFET data sheet. (Reprinted with permission of Siliconix inc.)

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Drain-Source Breakdown Voltage V_{GS} = 0, I_D = 250 µA	IRF350,352 IRF351,353	$V_{(BR)DSS}$	400 350	- -	- -	V
Gate Threshold Voltage V_{DS} = V_{GS}, I_D = 250 µA		$V_{GS(th)}$	2.0	-	4.0	
Gate-Body Leakage V_{DS} = 0, V_{GS} = ±20 V		I_{GSS}	-	-	100	nA
Zero Gate Voltage Drain Current V_{DS} = $V_{(BR)DSS}$, V_{GS} = 0		I_{DSS}	-	-	250	µA
Zero Gate Voltage Drain Current V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 0, T_J = 125°C		I_{DSS}	-	-	1000	
On-State Drain Current[2] V_{DS} = 10 V, V_{GS} = 10 V	IRF350,351 IRF352,353	$I_{D(on)}$	15 13	- -	- -	A
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A	IRF350,351 IRF352,353	$r_{DS(on)}$	- -	0.22 0.3	0.30 0.40	Ω
Drain-Source On-State Resistance[2] V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C	IRF350,351 IRF352,353	$r_{DS(on)}$	- -	0.5 0.6	0.60 0.80	
Forward Transconductance[2] V_{DS} = 15 V, I_D = 8.0 A		g_{fs}	8.0	9	-	S(℧)
Input Capacitance	V_{GS} = 0 V_{DS} = 25 V f = 1 MHz	C_{iss}	-	2700	3000	pF
Output Capacitance		C_{oss}	-	450	600	
Reverse Transfer Capacitance		C_{rss}	-	160	200	
Total Gate Charge	V_{DS} = 0.8 x $V_{(BR)DSS}$, V_{GS} = 10 V, I_D = 18 A (Gate charge is essentially independent of operating temperature)	Q_g	-	77	120	nC
Gate-Source Charge		Q_{gs}	-	14	-	
Gate-Drain Charge		Q_{gd}	-	39	-	
Turn-On Delay Time	V_{DD} = 180 V, R_L = 25 Ω I_D = 8.0 A, V_{GEN} = 10 V R_G = 4.7 Ω (Switching time is essentially independent of operating temperature)	$t_{d(on)}$	-	14	35	ns
Rise Time		t_r	-	30	65	
Turn-Off Delay Time		$t_{d(off)}$	-	54	150	
Fall Time		t_f	-	15	75	

SOURCE-DRAIN DIODE RATINGS & CHARACTERISTICS (T_J = 25°C unless otherwise noted)

PARAMETERS/TEST CONDITIONS		Symbol	Min.	Typ.	Max.	Units
Continuous Current	IRF350,351 IRF352,353	I_S	- -	- -	15 13	A
Pulsed Current[1]	IRF350,351 IRF352,353	I_{SM}	- -	- -	60 52	
Forward Voltage[2] I_F = I_S, V_{GS} = 0	IRF350,351 IRF352,353	V_{SD}	- -	- -	1.8 1.6	V
Reverse Recovery Time I_F = I_S, dI_F/dt = 100 A/µs		t_{rr}	-	300	-	ns
Reverse Recovered Charge I_F = I_S, dI_F/dt = 100 A/µs		Q_{rr}	-	2.0	-	µC

[1] Pulse width limited by maximum junction temperature (refer to transient thermal impedance data, figure 11)
[2] Pulse test: Pulse width ≤ 300 µsec, Duty Cycle ≤ 2%

Figure 7.11 (Continued).

With confidence, we believe that we have a power DMOSFET having the following maximum specifications: 400 V, 15 A, and 0.3 Ω. When we look with more discernment at the column of electrical characteristics (at T_C = 25°C), we find,

$$r_{DS(on)} = 0.3\ \Omega \text{ at } V_{GS} = 10\ V,\ I_D = 8.0\ A$$

What we are probably witnessing is a holdover from the power bipolar transistor era, when data sheets would offer a maximum collector current (I_C) and then characterize the remaining parameters at 1/2 I_C. But the informed reader may have a gnawing question, namely, Does the device still offer an $r_{DS(on)}$ of 0.3 Ω when I_D is 15 A? The answer is, "It may," since the component is, in all likelihood, conservatively rated at an I_D of 8 A.

Accidentally or otherwise, however, this holdover from tradition may be covering a debilitating effect known as the *pinch resistance*. This is identified in the power DMOSFET equivalent circuit (Figure 5.10) as a JFET in *series with the drain*. Careful comparison of Figure 5.10, with the cross-sectional view provided in Figure 1.18 (keeping in mind the form of the JFET from Figure 2.1), should offer the reader insight as to how the JFET enters into the circuit as a pinch resistor. The equivalent source terminal of this *pinch-FET* lies immediately beneath the oxide—along the path of the channel region—whereas its equivalent drain terminal merges into the epi region. The gate is the *p-well body diffusion*. This pinch-FET exhibits characteristics similar to any JFET, including saturation. As the drain current rises (for the power DMOSFET as well as for the parasitic JFET), we discover, as we saw in Figure 2.2, that as we approach I_{DSS}—current *saturation* for the parasitic JFET—the channel resistance rises. This is the pinch resistor effect. If the power DMOSFET suffers from this effect, we should expect to see a nonlinear increase in $r_{DS(on)}$ with increasing drain current. If the specification $V_{DS(on)}$ (otherwise known as V_{SAT}) is provided on the data sheet at the full-rated current $I_{D(on)}$, or perhaps even at I_D, a simple manipulation of Ohm's law will allow you to detect whether the pinch resistance r_p, exists at this current level. The effect is shown in Figure 7.12:

$$r'_{DS(on)} = r_{DS(on)} + r_p = \frac{V_{DS(on)}}{I_{D(on)}} \qquad (7.7)$$

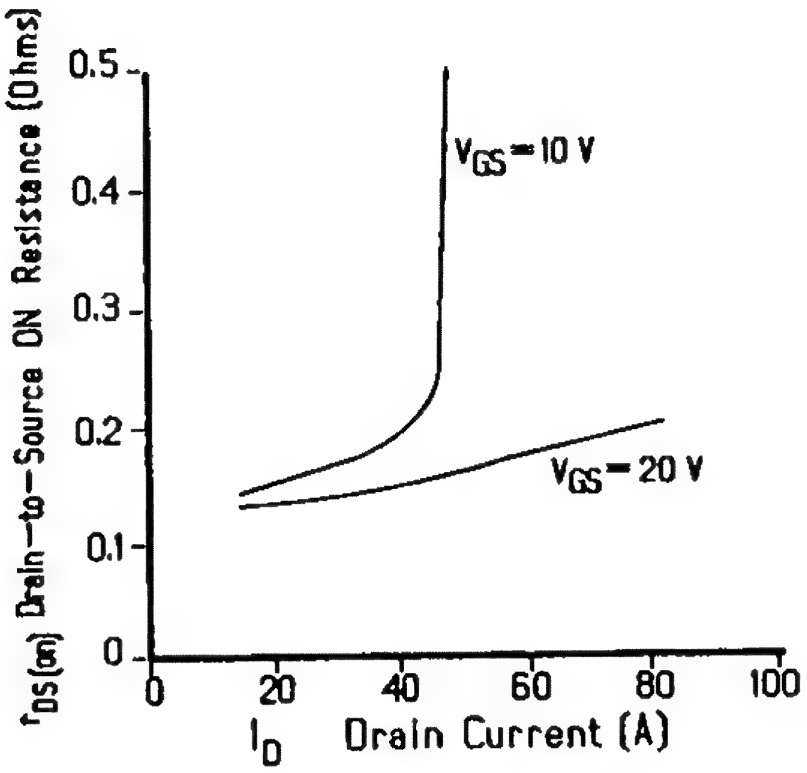


Figure 7.12 The effect of the pinch resistance on overall drain-to-source resistance as the operating drain current rises. Heavily enhancing the channel with excessive gate voltage helps to overcome the effect.

where the primed value $r'_{DS(on)}$ identifies the *total* ON resistance of the power DMOSFET at full-rated drain current.

In Chapter 3, we learned that the absolute maximum continuous drain current is a *calculated* value based on the power dissipation and the ON resistance at maximum junction temperature (see Eq. 3.1). It is not a measured value.

Some data sheets identify this absolute maximum current as plus or minus a given value. This does not imply that the power DMOSFET is bidirectional; it only means that the body-drain diode is capable of handling the same magnitude of current as the enhanced channel, which should come as no surprise. Actually the diode current can be considerably greater than the channel current when we consider the area of the pn region. Diode-current flow is always the reverse of drain-current flow (remember I_D and I_S in Chapter 3), hence the ± polarity.

Why, then, do some vendors show this dual polarity? Possibly to remind users that the body-drain diode has application as a clamp diode.

Another absolute maximum specification that needs explanation is the pulsed drain current. By definition it is, as stated, a

pulsed measurement. But we need to exercise caution, for it is *not* necessarily representative without a careful appreciation of the accompanying maximum safe operating area (SOA) graph (see Figure 5.14). We need to ask whether this pulse test is a single, nonrepetitive pulse, or, in fact, a series of pulses of some pulse-repetition frequency (PRF). Hopefully the data sheet will answer our question. Furthermore, we may need to ask at what voltage this pulsed drain current is measured. The SOA graph provides us with clear answers. For example, if the IRF350 data sheet indicates that the pulse width is less than 300 μs, then a V_{DS} of 70 V is about as high as we dare go. Yet we must proceed with caution when using the SOA curves to arrive at definitive answers simply because these curves apply only to a *single pulse* at a case temperature (T_C) of 25°C. Not particularly practical!

On the other hand, possibly because of our application, we may want to know the allowable pulse width *and PRF*. A more useful graph, the transient thermal impedance curves (see Chapter 6) on the data sheet should offer answers, since chip temperature is affected.

If this transient thermal impedance curve does not exist for our selection and we wish to use the power DMOSFET in a pulsed-power mode, we would be best advised to select a different FET for which this curve is available on the data sheet.

An important but seldom disclosed specification that ought to accompany I_{DM} is $V_{DS(on)}$—the peak-current saturation voltage. At high peak currents, if the pinch-resistance effect does occur (and it most surely will), the high $V_{DS(on)}$ may be a surprising discovery! Indeed, if $V_{DS(on)}$ is greater than your supply voltage, you will most assuredly not reach I_{DM}! Testing a power DMOSFET for its peak-current saturation voltage often helps to differentiate one vendor's product from another having the same part number, as illustrated in Figure 7.13.

A more useful plot might be to emulate that of the switching bipolar transistor's $V_{CE(sat)}$ versus base current I_B, but substitute $V_{DS(on)}$ for $V_{CE(sat)}$ and V_{GS} for I_B, as shown in Figure 7.14.

Proceeding with our power DMOSFET data sheet specifications, we stop at $V_{BR(DSS)}$ (or BV_{DSS}) where, invariably, the test conditions identify a drain current equal to the permissible maximum leakage current I_{DSS}, which, in turn, is specified at the breakdown voltage! The specifications for breakdown voltage and leakage current are complementary. Each upholds the other—but only at 25°C.

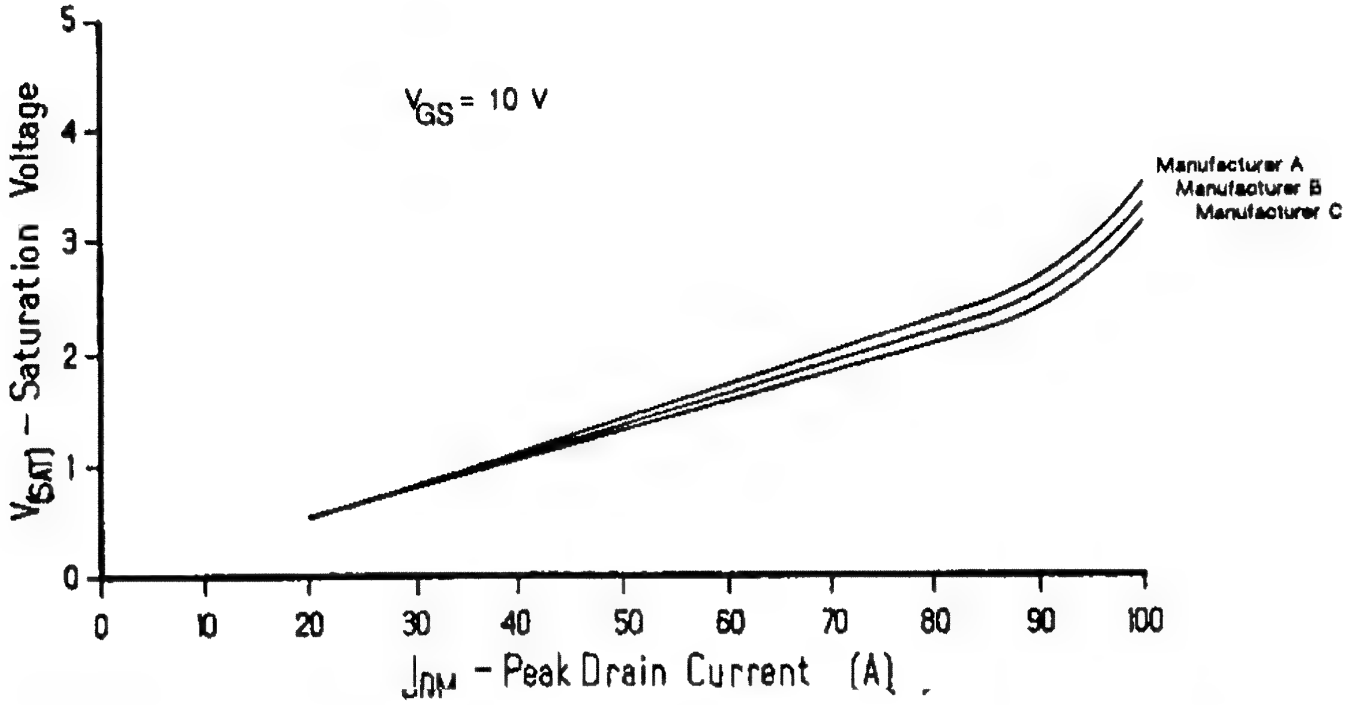


Figure 7.13 Variation in V_{SAT} between power DMOSFETs having the same part number but coming from different vendors helps to identify the effects of the "hidden" pinch-FET.

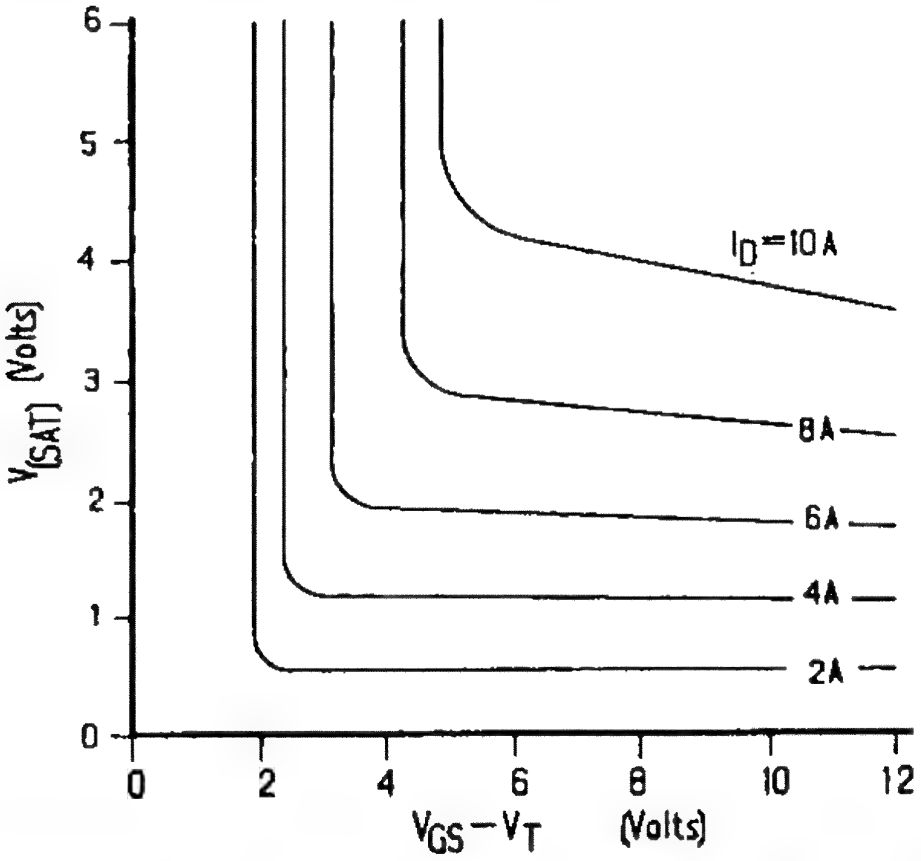


Figure 7.14 Drain output characteristics showing saturation at various drain currents and gate drive levels; gate drive normalized to V_T.

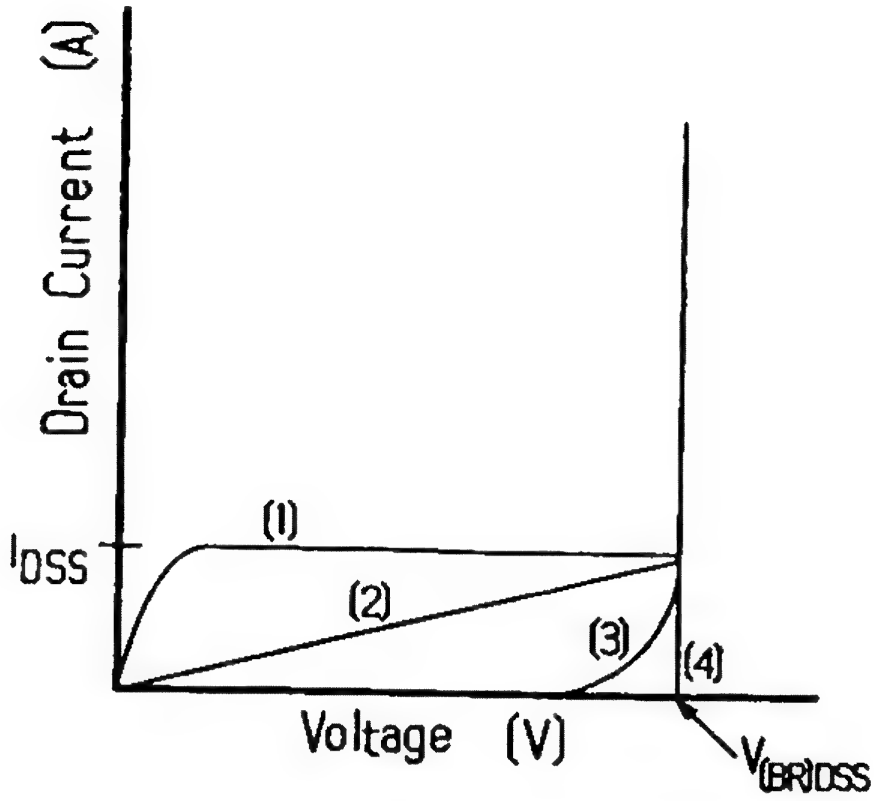


Figure 7.15 The four possible breakdown voltage scenarios for an enhancement-mode MOSFET: (1) current rising immediately to the maximum allowable leakage, (2) current slowly rising to the maximum allowable leakage, (3) the characteristic "soft" breakdown, and (4) the desired optimum breakdown.

The fault with these complementary specifications is that the FET under consideration could have any of four breakdown characteristics, as shown in Figure 7.15. To ensure a sharper breakdown characteristic, it would be especially welcome to have I_{DSS} specification, given, as it is, at the breakdown voltage, but perhaps at one-quarter the breakdown test current.

An important parameter is the gate threshold voltage $V_{GS(th)}$ specification, found on every enhancement-mode MOSFET data sheet. It is this parameter that identifies whether our n-channel device is, or is not, compatible with transistor-to-transistor logic (p-channel devices, by definition, are not TTL compatible, since TTL logic is *positive*-going; viz., +0.8 V to +2.4 V).

We must not forget that the voltages specified for threshold do not represent the true threshold voltage of the device. SPICE II modeling information is not currently available from the JEDEC-registered data sheet.

"Logic compatibility" is often a difficult term, having different meanings for different applications. Using our example (the

IRF350), we could guarantee, worst-case, that 5 V logic could achieve 1 ampere of drain current at 25°C. We could not guarantee that +2.4 V TTL logic would even turn on the power DMOSFET.

Likewise, it is the influence on $V_{GS(th)}$ that determines whether our power DMOSFET is "rad hard," or resistant to nuclear radiation. Ionizing radiation affects the threshold voltage by introducing charges into the gate oxide, which causes the magnitude of $V_{GS(th)}$ to diminish (go more negative). For an n-channel, enhancement-mode MOSFET, this means that at the radiation level eventually reached, the device is ON even when $V_{GS} = 0$! On the other hand, a p-channel MOSFET becomes increasingly more OFF as the threshold increases.

Increasing chip temperature also forces the threshold down (typically from −3 to −6 mV/°C), meaning that for the n-channel device, the MOSFET may turn ON sooner than expected. If the FET is OFF, the chip temperature is affected directly by the ambient temperature. Once the FET is ON, the combination of the downward threshold drift and rising $r_{DS(on)}$ (with increasing temperature) will reach a point of equilibrium that is commonly recognized as the zero TC. At the zero TC, the downward drift of $V_{GS(th)}$ is matched by the rising $r_{DS(on)}$.

The transfer curves on the data sheet should show performance at −55, 25, and +125°C. Zero TC may occur either in the square-law region or in the velocity-saturation region. Predicting where is not easy. Be forewarned that these transfer curves result from *pulsed* measurements and that these three temperatures, therefore, reflect the ambient, case, and chip temperatures ($T_A = T_C = T_J$). In actual practice we must be reminded that for all practical purposes, the temperature is T_J. Therefore, to use these data for purposes other than pulse we need to first define the true *operating* chip temperature (see Chapter 6). Yet, if we plan to use the power DMOSFET only as a switch, of what use is g_{fs}? Since, as we learned earlier, for a short-channel FET (like the DMOSFET), once we have fully turned ON the FET, V_{GS} has little effect on transconductance. Unlike the small-signal JFET, g_{fs} does *not* reflect on the value of $r_{DS(on)}$.

Continuing our review of the electrical characteristics, on the typical non-JEDEC-registered data sheet we find the specification $I_{D(on)}$ offered as a *minimum* current. This parameter is generally not found on JEDEC-registered data sheets. For the majority of cases, this minimum value of $I_{D(on)}$ *equals* the absolute maximum value of I_D. Note, however, that $I_{D(on)}$

always represents a pulsed measurement, whereas I_D is rated as a continuous current. What $I_{D(on)}$ proves to us is that the power DMOSFET can achieve the maximum continuous current (I_D) at the rated gate-source voltage V_{GS}, at 25°C. What the data sheet fails to assure us is that we can successfully reach I_{DM}, regardless of gate voltage. Some manufacturers offer a supplemental curve of $r_{DS(on)}$ versus I_D that extends to I_{DM}. As an added benefit, this curve (Figure 7.12) offers insight into the effect of high operating currents on the pinch resistance.

Reading power MOSFET data sheets published since 1988, we observe several charge parameters (Q). For switching applications these charge parameters will eventually replace the more common capacitance parameters (such as C_{iss}) and the somewhat useless parameter C_{rss}.

If we pick up the derivations of Eqs. 3.7 to 3.9, we find:

$$\frac{Q}{dt} = \frac{C\ dV}{dt} \tag{7.8}$$

or

$$C = \frac{Q}{dV} \tag{7.9}$$

Equation 7.9 may be rewritten as follows:

$$C_{iss} = \frac{Q_{g(th)}}{dV} \tag{7.10}$$

Reverse transfer capacitance, C_{rss}, is more difficult to derive from the charge data. However, for most switching applications, knowing the specific value of C_{rss} is of little importance because the effects of the Miller capacitance may be taken either from the charge characteristics Q_{dg} on the data sheet or, possibly with some difficulty, from the charge curves (Figure 5.5) that accompany a well-organized data sheet.

An additional specification that has recently been found on power DMOSFET data sheets is $I_{A(R)}$—repetitive (optional) avalanche current. This test is better known as the UIS or unclamped inductive switching test (see Chapter 3). Although certainly current is important, we must not fall into the emotional trap thinking that the higher the current level, the better.

Another specification that has caused considerable anguish is t_{rr}—reverse recovery time of the parasitic body-drain diode.

Truly, the smaller the value the better. All data sheets offer only a typical value, so it is incumbent on the user to find the shortest time *if this specification is of importance.*

Reverse recovery time is important whenever the application forces a reverse current through the DMOSFET: that is, whenever I_S is forced. Such often occurs in H-bridge motor drives or H-bridge drives to inductive loads. For such applications, switching times are really a function of t_{rr}, *not* $t_{d(off)}$ or t_f.

REFERENCE

Richman, Paul (1973). *MOS Field-Effect Transistors and Integrated Circuits.* John Wiley & Sons, New York.

8

The Many Ways to Power Up FETs

8.1 Introduction

The FET, like the resistor, the capacitor, and the operational amplifier, is a basic building block. It is found in practically every electronic circuit either individually or as an active element within an integrated circuit. Because of its universality, we could not hope to be exhaustive if we attempted to tackle even some of the design problems.

Consequently, this chapter does not focus on design. Here we touch on how to bias FETs to achieve the desired operational characteristics. The few references that close this chapter offer the reader some design support.

Within the family of FETs, as we remember from Figure 1.1, there are two modes of operation: depletion and enhancement. Regardless of type, style, or the novelty of construction, at zero bias ($V_{GS} = 0$), the depletion-mode FET is normally ON and the enhancement-mode FET is normally OFF. The n-channel operates with a positive potential at its drain, whereas the p-channel performs with its drain more negative than its source.

By now we are familiar with the operational differences of the FET as compared with the bipolar transistor. Whereas the bipolar transistor operates by the injection of base *current*, the FET is controlled by a gate *voltage*. Because the FET is voltage-controlled, the gate may offer a high input resistance as compared to the current-controlled base of the bipolar transistor.

8.2 Powering Up the Small-Signal JFET

A cursory examination of any JFET data sheet shows several wide parameter variations. Gate-source cutoff voltage, $V_{GS(off)}$, saturation drain current, I_{DSS}, forward transconductance, g_{fs}, and/or ON resistance, $r_{DS(on)}$, are among the worst offenders.

In most production environments we must be prepared to use JFETs exhibiting wide-ranging parameters. It is not unusual to find the specifications for $V_{GS(off)}$ and I_{DSS} spanning 3:1 or greater. Some JFET specifications may span 8:1, or even 10:1!

Because of the wide disparity of parameters found on most JFET data sheets, we need to be especially familiar with the proper biasing methods to achieve our desired design objectives. In developing the proper biasing, it is very helpful to select the JFET whose data sheet offers typical performance curves at the parameter limits. The example provided in Figure 8.1, for the 2N4867-series, greatly eases the task (compare Figure 8.1 with Figure 7.2). Note that output characteristics are provided for $V_{GS(off)}$ of -0.5, -1.0, -2.3, and -3.0 V. The transfer characteristic curves span from a V_{GS} of -0.5 to -4.2 V (at 25°C), entirely adequate to develop proper biasing for the 2N4867 series for practically any service for which the FET was designed.

When working with JFETs, it is convenient to have at your fingertip the various mathematical relationships that might help resolve unknown parameters.

Assuming, as we generally have, that the JFET follows Shockley's equation, we use the equation to calculate drain current I_D as a function of gate bias V_{GS}:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^K \qquad (8.1)$$

We can calculate drain voltage V_{DS} at which drain current I_D saturates by the following approximation:

$$V_{DS} \approx V_{GS(off)}\left(\frac{I_D}{I_{DSS}}\right)^{1/2} \qquad (8.2)$$

A frequent application is to use the JFET as a voltage-controlled resistor (VCR). To approximate this resistance in the triode region:

PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

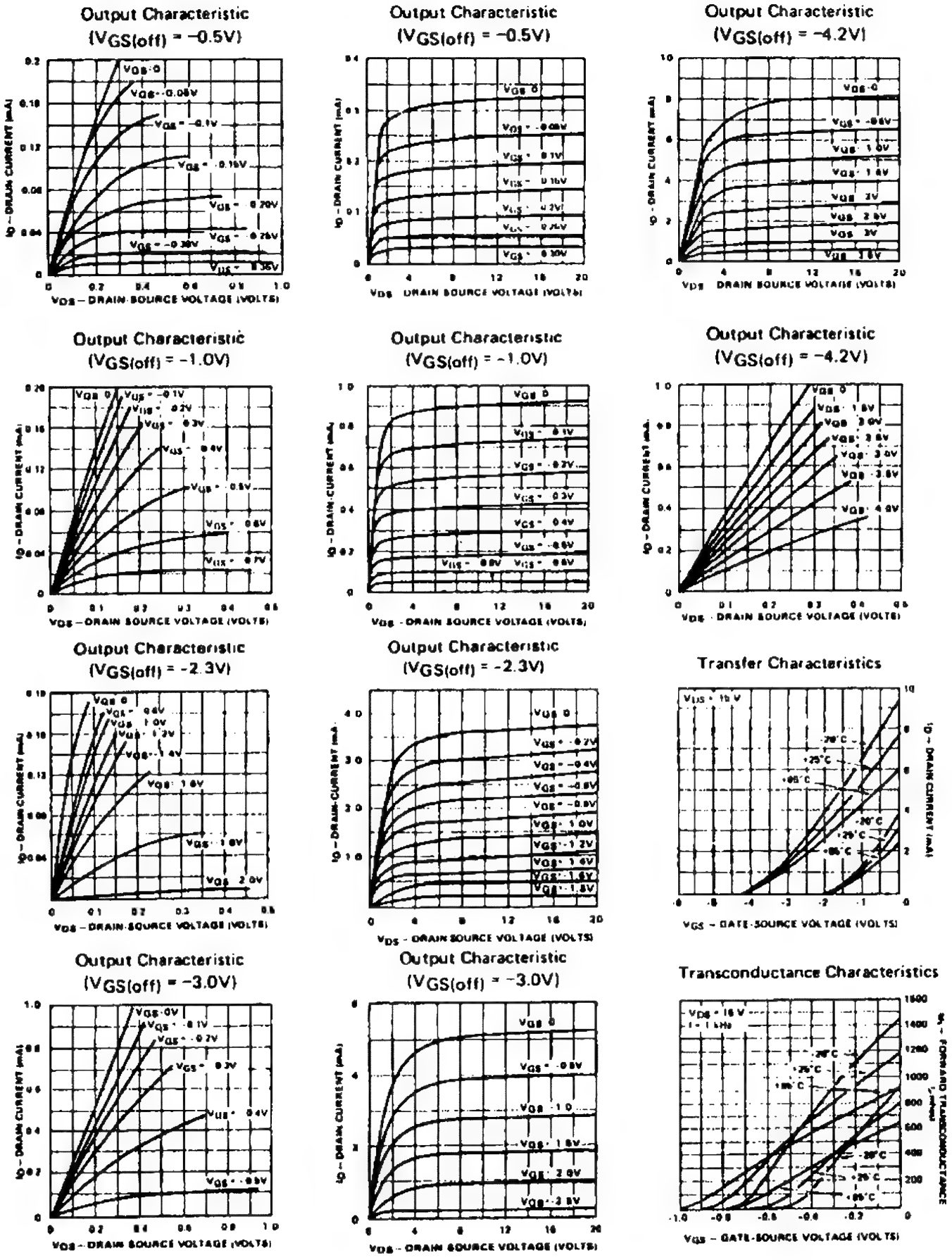


Figure 8.1 Transfer and output characteristic curves for the 2N4867 series JFET

$$r_{DS} = \frac{|V_{GS(off)}|^2}{KI_{DSS}(V_{GS(off)} - V_{GS})} \tag{8.3}$$

A term not defined in Chapter 3—transconductance at zero gate bias—may be calculated as follows:

$$g_{fso} = \frac{KI_{DSS}}{V_{GS(off)}} \tag{8.4}$$

Likewise, transconductance at any bias may be calculated as follows:

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \tag{8.5}$$

Gate-source cutoff voltage also is related by:

$$V_{GS(off)} = \frac{K\ I_{DSS}}{g_{fso}} \tag{8.6}$$

In all the equations above, we may let K = 2.

A close approximation of the zero temperature coefficient (0 TC) may be derived (but *not* from Shockley's equation):

$$I_{DZ} = I_{DSS}\left(\frac{0.63}{V_{GS(off)}}\right)^2 \tag{8.7}$$

8.2.1 Biasing for Amplifier Service

The problem of wide parameter variations becomes immediately apparent when we construct a dynamic load line to initiate our design of a Class A amplifier stage. Which output characteristic is typical for the JFET? Obviously, as we examine the data sheet, the answer is "More than one!" For example, using the data sheet for the 2N4868 (Figure 7.2), the limits of $V_{GS(off)}$ span from −1.0 to −3.0 V, and I_{DSS} from 1 to 3 mA. Fortunately, using the typical output-characteristic performance curves that represent this JFET (Figure 8.1) we can select and super-

impose those for a $V_{GS(off)}$ of −1.0 and −3.0 V, as shown in Figure 8.2.

At least three popular biasing methods have found wide use. These are:

Constant-voltage biasing (see Figure 8.3a), especially useful when using very low values of d-c drain resistors common in high-frequency amplifiers, where transformer coupling is frequently used

Constant-current biasing (see Figure 8.3b), particularly suited in low-drift, d-c amplifier service using differential pairs

Self-biasing (see Figure 8.3c), a widely used method that greatly simplifies a-c amplifier design

Regardless of which type of biasing we select, the operating point of the JFET—the "Q" point—is based on the sort of performance we expect of the JFET. That is, are we designing a linear amplifier, a high-gain amplifier, an oscillator? Whatever our design, it is important that V_{DS} be sufficiently greater than V_p to ensure that the JFET is operating in its saturation (or pinch-off) region.

Earlier, we discovered that Shockley's equation (Eqs. 2.2, 4.2, and 8.1) identifies a relationship between V_{GS} and I_D. The operating Q-point we establish with bias, V_{GSQ}, which, in turn, produces the quiescent drain current, I_{DQ}. If we do not make use of the characteristic curves offered by most vendors (as we see in Figure 8.1 and 8.2), our design may produce widely varying results!

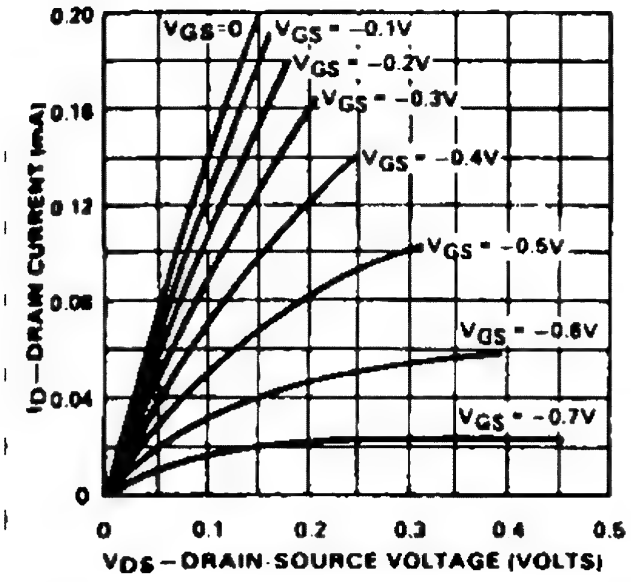
An excellent biasing scheme that is somewhat more costly involves using a constant-current source as shown in Figure 8.3b. Although widely used to bias differential pairs, it is an especially popular biasing scheme for source followers, as shown in Figure 8.4.

Summarizing a few basics, Figure 8.5 identifies both the circuits and equations for the three principal JFET circuits: common source, source follower, and common gate.

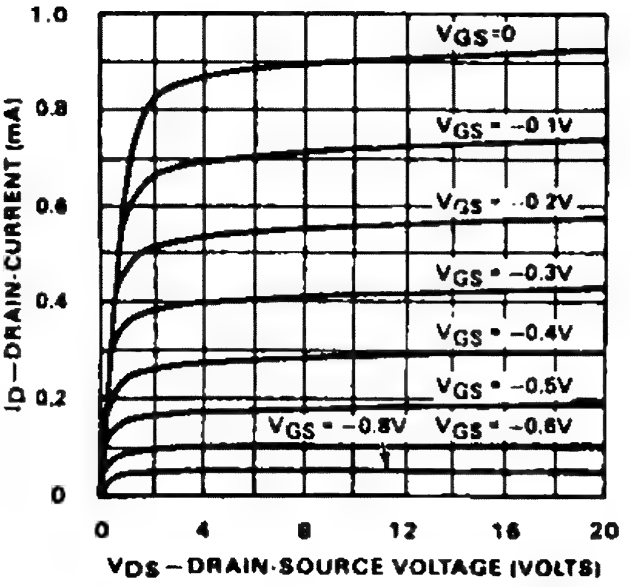
Designing high-frequency amplifiers requires an additional manipulation of stability factors (both Linvill for device stability, and Stern, for circuit stability), which the reader is encouraged to check in the references concluding this chapter.

The differential pair, to be completely effective, must be operated at the data-sheet-prescribed drain current to ensure both the offset and drift specifications, as well as common-mode rejection ratio (CMRR), if this specification is offered on the

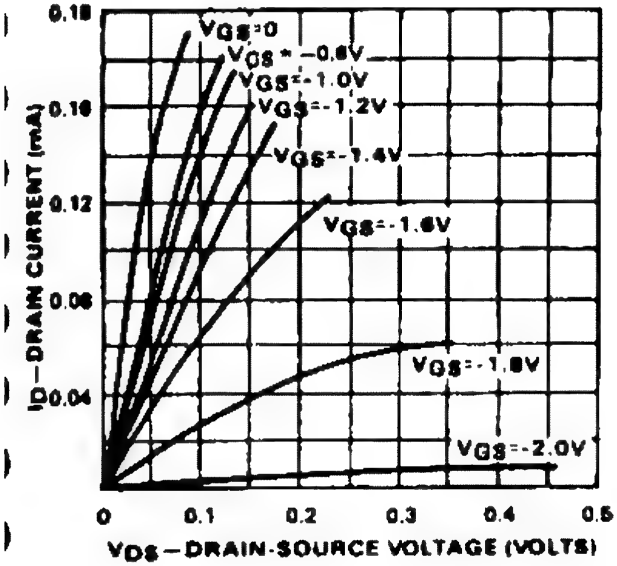
Output Characteristic
($V_{GS(off)}$ = −1.0V)



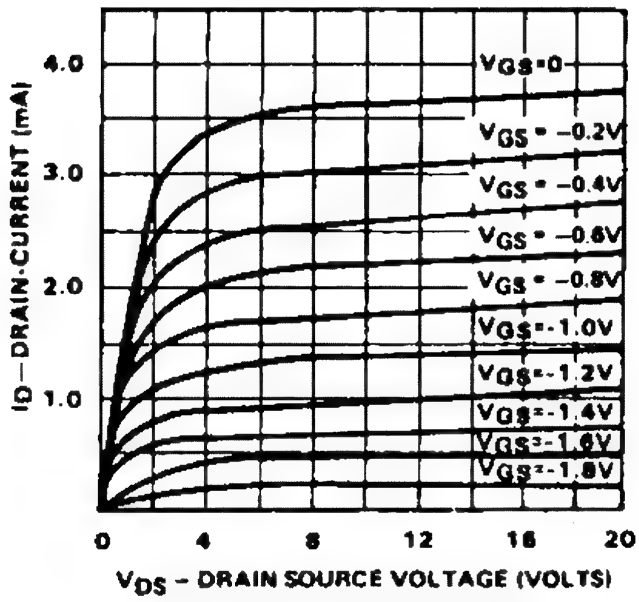
Output Characteristic
($V_{GS(off)}$ = −1.0V)



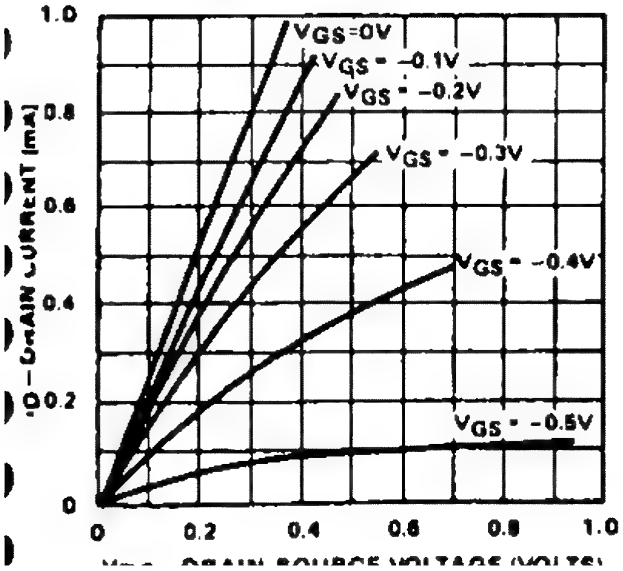
Output Characteristic
($V_{GS(off)}$ = −2.3V)



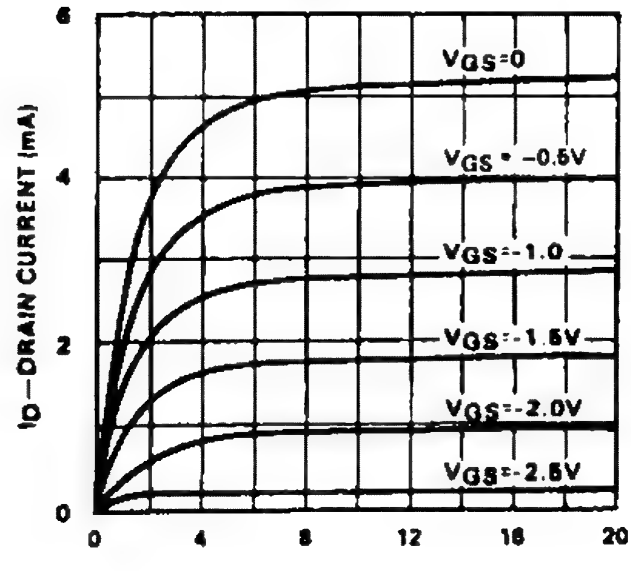
Output Characteristic
($V_{GS(off)}$ = −2.3V)



Output Characteristic
($V_{GS(off)}$ = −3.0V)



Output Characteristic
($V_{GS(off)}$ = −3.0V)



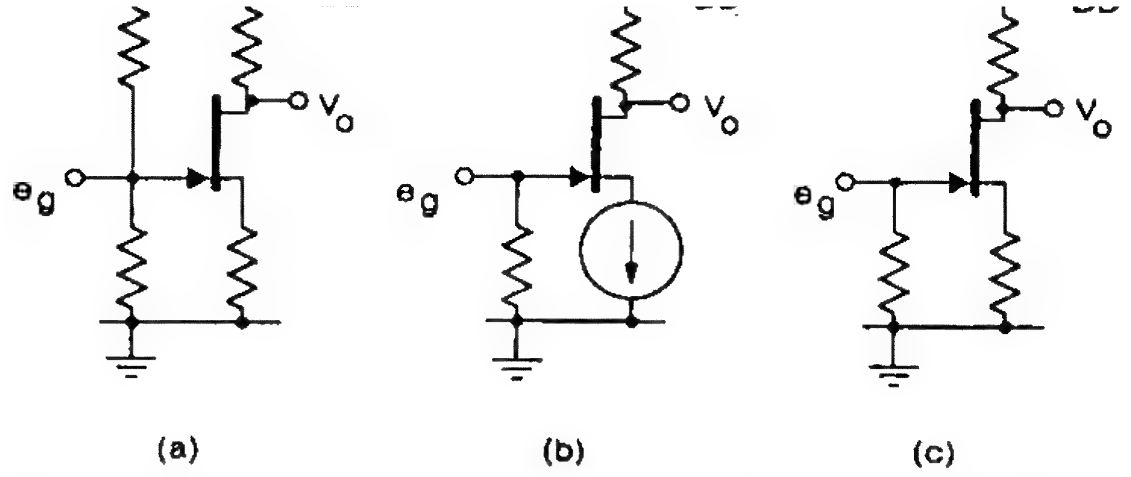


Figure 8.3 (a) Constant-voltage biasing for JFETs. Note the resistor voltage divider that establishes the gate potential. (b) Constant-current biasing for JFETs. A current regulator sets the drain current. This fixes the output voltage for any load. Bypassing the current regulator will lower the stage gain. (c) Self-biasing. Bypassing the source resistor will increase the gain of the circuit.

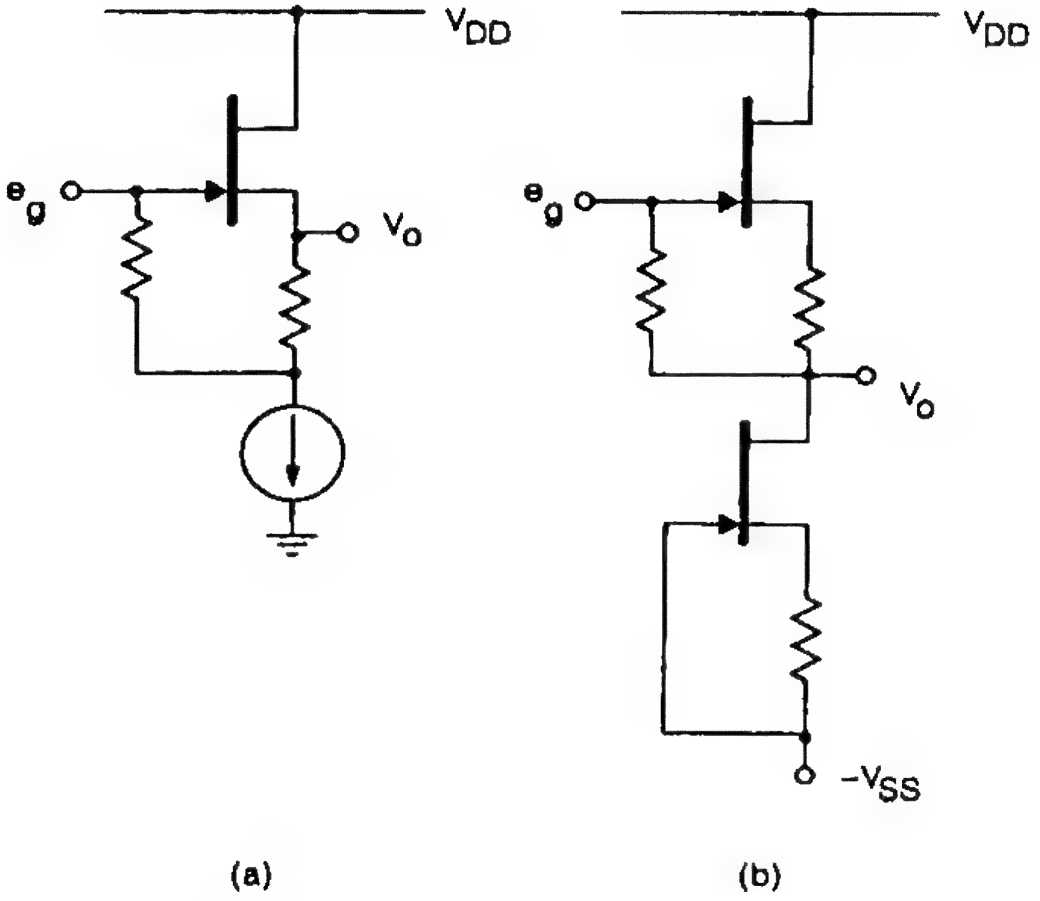
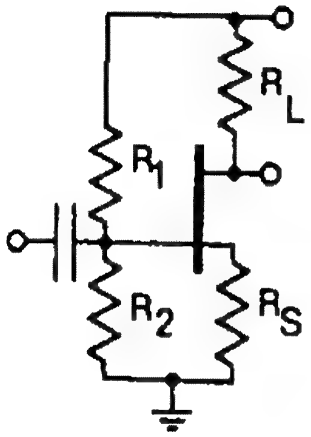


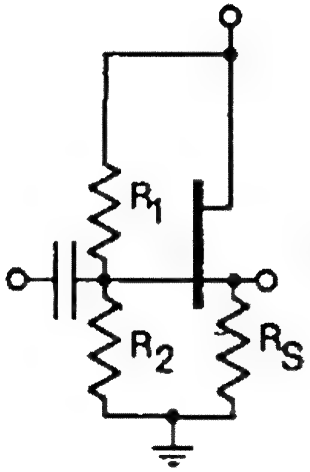
Figure 8.4 Constant-current biasing of source followers in which (a) a current source is used to improve stability and (b) a pair of matched JFETs serves this purpose. The input-output offset may be set at zero. The source resistors may be selected to set the performance at or near the specified zero temperature coefficient operating drain current.



(a)

	EXACT	ASSUMPTIONS for APPROXIMATE SOLUTIONS	
VOLTAGE GAIN	$A_V = \dfrac{-g_{fs}\ R_L}{1+g_{os}(R_L + R_S)\ +g_{fs}R_S}$	$g_{os}(R_L+R_S) \ll 1$	$A_V \approx \dfrac{R_L}{\frac{1}{g_{fs}} + R_S}$
INPUT IMPEDANCE	$Z_{in} = R_g \Vert \dfrac{\frac{1}{g_{is}}}{1-\frac{g_{fs}\ R_S}{1+g_{os}(R_L+R_S)+g_{fs}R_S}}$	$g_{os}(R_L+R_S) \ll 1$	$Z_{in} \approx R_1 \Vert R_2$
OUTPUT IMPEDANCE	$Z_o = \dfrac{1 + R_S(g_{os}+g_{fs})}{R_L g_{os} + 1 + R_S(g_{os}+g_{fs})}$	$g_{os}(R_L+R_S) \ll 1$	$Z_o \approx R_L$

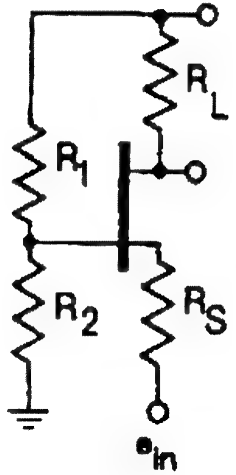
Figure 8.5 (a) Operating basics for the common-source JFET amplifier. (b) Operating basics for the JFET source follower. (c) Operating basics for the JFET common-gate amplifier.



(b)

	EXACT	ASSUMPTIONS for APPROXIMATE SOLUTIONS	
VOLTAGE GAIN	$A_V = \dfrac{g_{fs} R_S}{1 + R_S (g_{fs} + g_{os})}$	$R_S (g_{fs} + g_{os}) \ll 1$	$A_V \approx \dfrac{R_S}{\frac{1}{g_{fs}} + R_S}$
INPUT IMPEDANCE	$Z_{in} = R_g \parallel \dfrac{\frac{1}{g_{fs}}}{1 - \frac{g_{fs} R_S}{1 + R_S (g_{fs} + g_{os})}}$	$R_g \gg \dfrac{\frac{1}{g_{is}}}{1 - g_{fs} R_S}$	$Z_{in} \approx R_1 \parallel R_2$
OUTPUT IMPEDANCE	$Z_o = \dfrac{R_S + g_{fs} R_S^2}{1 + R_S (g_{fs} + g_{os})}$	$g_{os} \to 0$	$Z_o \approx R_S \parallel \dfrac{1}{g_{fs}}$

Figure 8.5 (Continued).



(c)

	EXACT	ASSUMPTIONS for APPROXIMATE SOLUTIONS	
VOLTAGE GAIN	$A_V = \dfrac{g_{fs}\ R_L}{1+g_{os}(R_L + R_S) + g_{fs}\ R_S}$	$g_{os}(R_L + R_S) \ll 1$	$A_V \approx \dfrac{R_L}{\frac{1}{g_{fs}} + R_S}$
INPUT IMPEDANCE	$Z_{in} = \dfrac{1}{g_{fs}+g_{os}} + (R_S+R_L)\dfrac{g_{os}}{g_{os}+g_{fs}} + \dfrac{R_S\, g_{fs}}{g_{os}+g_{fs}}$	$g_{os} \ll g_{fs}$ $g_{os}(R_L + R_S) \ll 1$	$Z_{in} \approx R_S + \dfrac{1}{g_{fs}}$
OUTPUT IMPEDANCE	$Z_o = \dfrac{R_L}{\frac{g_{os}(R_L + R_S)}{1 + g_{fs}\ R_S} + 1}$	$g_{os}(R_L + R_S) \ll 1$	$Z_o \approx R_L$

Figure 8.5 (Continued).

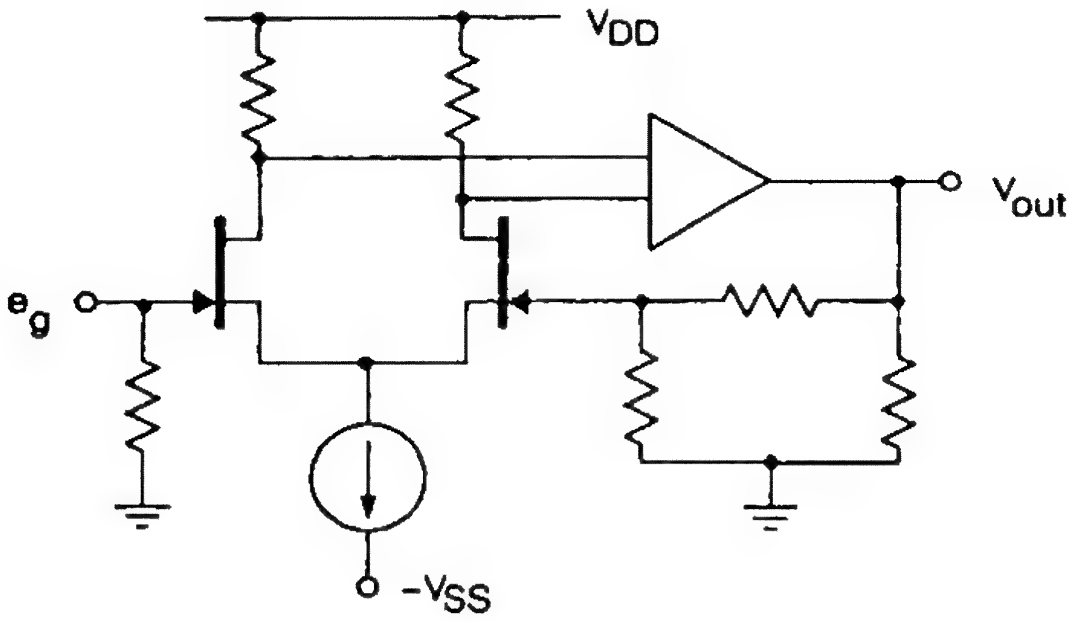


Figure 8.6 Schematic for a JFET-input operational amplifier.

data sheet. There is no better means than to use a "long-tailed pair" dual JFET tied to a constant-current source, as shown in Figure 8.6 for the JFET-input operational amplifier. Keep in mind that the constant-current source must pass the current of *both* JFETs. Optimum performance is best attained when operating from balanced rails (viz., ± same magnitude of voltage), where the dual JFET sources are at zero potential with respect to the common ground (greatly simplifying the gate biasing). Referring to Figure 8.6, we have 15 V across the constant-current source (Motorola 1N5313 or Siliconix CR430 at 430 μA) and 15 V across the combined JFET and load resistance. To further ensure proper operation of the dual JFET, we establish a drain voltage V_{DS} sufficient to keep operation in the saturation region. Half the rail voltage (7.5 V) should do this nicely, the load resistors and the JFET sharing equally:

$$R_{L1} = R_{L2} = \frac{E}{I} = \frac{7.5}{215 \times 10^{-6}} \approx 35\ k\Omega \qquad (8.8)$$

where $215 \times 10^{-6} = 430\ \mu A/2$.

Voltage gain for the differential amplifier is the same as for a single common-source stage:

$$A_V = \frac{g_{fs} R_L}{1 + g_{os} R_L} \qquad (8.9)$$

An interesting exercise shows the advantage of using a constant-current diode in the common source of the long-tailed pair dual:

$$A_{CM} = \frac{g_{fs}R_L}{1 + 2g_{fs}R_S} \qquad (8.10)$$

where R_S is the value of the common-source resistor. We can immediately see that if R_S is high, then A_{CM} is low. The lower the better (preferably zero!).

8.2.2 Biasing for Switching Service

Often JFETs are pressed into service as analog switches where the input signal rises and falls symmetrically about a fixed reference, which may or may not be at ground potential. If we remember the relationship between $r_{DS(on)}$ and V_{GS} (Eq. 8.3), we should not be surprised to learn that performance is acutely dependent on both gate bias and signal amplitude. For an example, let us take the 2N4392 that we examined in Chapter 7.

	Min	Max
$V_{GS(off)}$	−2	−5 V
$r_{DS(on)}$	—	60 Ω

The 2N4392 is used as a simple series-connected, single-pole, single-throw (SPST) switch driven indirectly from ± rails (Figure 8.7). Can you explain the following matrix? (*Hint*: Assume that we can turn the SPST switch full ON or full OFF. Check what gate bias will ensure an OFF condition.)

Rail voltages	Analog voltage range
−15 V +15 V	−10 to +15 V
−10 V +20 V	−5 to +20 V
−12 V +12 V	−7 to +12 V

To ensure a full OFF condition when the JFET gate is biased beyond cutoff, we must remember that gate bias is *always* refer-

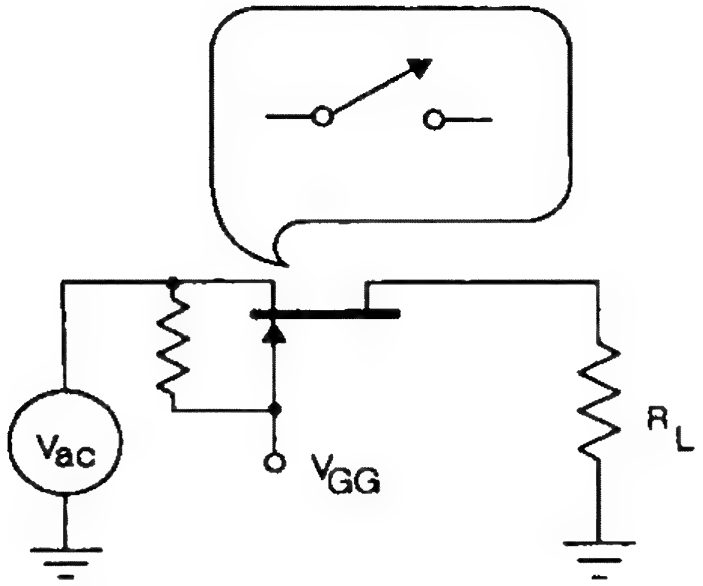


Figure 8.7 The simple series-connected JFET switch.

enced to the source. Consequently, if the analog signal—impressed on the source of this n-channel JFET—swings negatively to where the gate-to-source voltage V_{GS} is less than $|V_{GS(off)}|$ the JFET will turn ON! The analog switch offered in our example is powered from the rails. The only negative bias must come from the negative-polarity rail. Since we must ensure cutoff (for an OFF-state condition), the analog signal is limited to 5 V above the negative rail (check $V_{GS(off)}$ for the 2N4392).

JFETs in digital circuits must respond to zeros and ones, which often originate from either TTL or CMOS. A logic-compatible JFET circuit presents a challenge to the designer. A JFET is full ON at zero gate-source bias (logic 0). Unfortunately, an n-channel JFET is *still* ON at logic 1!. However, a p-channel JFET turns OFF when its gate bias rises *above* $V_{GS(off)}$; so if we select a low $V_{GS(off)}$ p-channel JFET, we may succeed in establishing a logic-compatible JFET circuit. The successful circuit, using the p-channel JFET, may operate as a level shifter or logic gate, as shown in Figure 8.8. But to be successful we must select a JFET whose $V_{GS(off)}$ is less than the logic 1 level. For +5 V logic, the 2N5116, having a $V_{GS(off)}$ maximum of +4 V, may be the right choice.

8.3 Powering Up the Small-Signal MOSFET

As we have learned, the MOSFET may be constructed to perform either as a depletion-mode or as an enhancement-mode transistor.

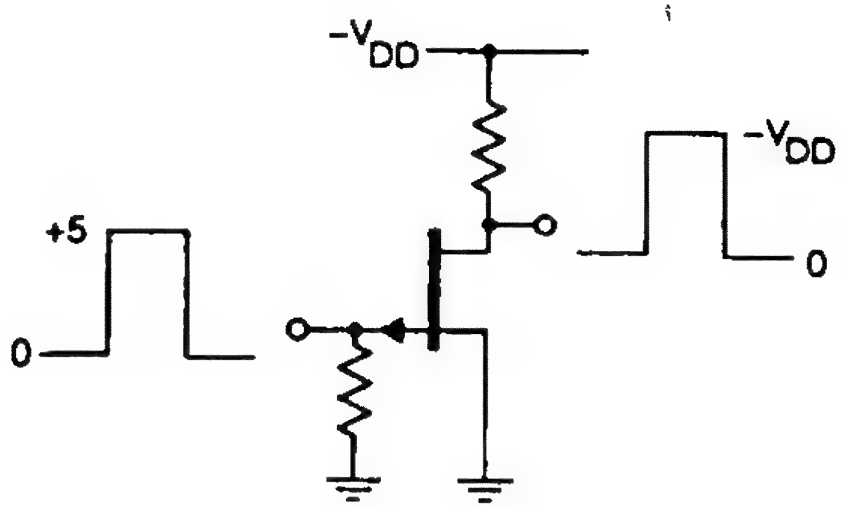


Figure 8.8 A low $V_{GS(off)}$ p-channel JFET performs like a logic gate or level shifter.

Furthermore, should we use a depletion-mode transistor, we can bias it into enhancement (see Figure 1.10). If the gate is not zener protected against electrostatic discharge (ESD), we may allow the gate voltage to swing both positively and negatively with respect to the source. No gate current can or will flow. At zero gate voltage, the depletion-mode MOSFET is normally ON, whereas the enhancement-mode MOSFET is OFF.

For the most part, biasing the small-signal MOSFET closely follows the rules just given for the JFET. Naturally, we need to realize that the enhancement-mode MOSFET may be biased directly from the same source as V_{DD}.

Whereas the JFET is a three-terminal device (source, drain, and gate), the MOSFET has at least *four* terminals, the fourth being the body. Many small-signal MOSFETs and all large-signal (power) DMOSFETs have the body terminal bridged internally (on the chip) to the source. If the body is *not* bridged internally but exists as a terminal—remembering that the body can act as a pseudo-gate (see Figure 5.8)—it is often *critically* important to the performance of the MOSFET that it be back-biased to the greatest potential the MOSFET will experience. That is, for the n-channel MOSFET, the body should be biased negatively; for the p-channel, positively. The body effect is best observed in Figure 8.9, which shows all the characteristics of the JFET's operating gate current that we saw earlier in Figure 4.8.

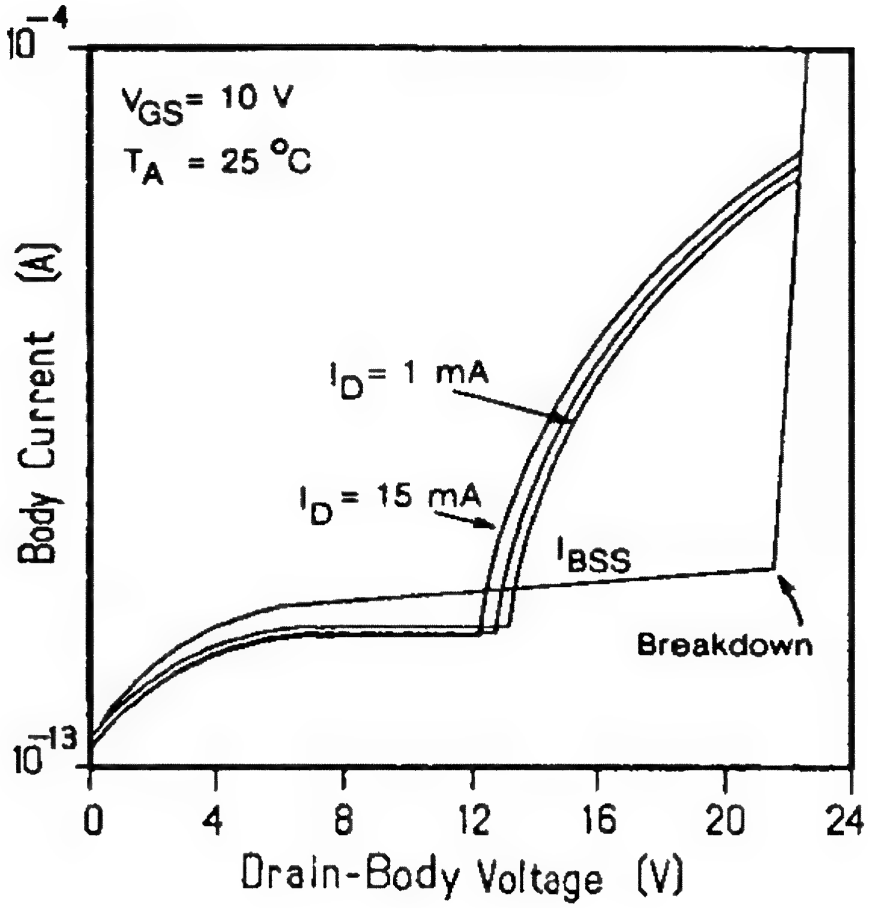


Figure 8.9 The body, acting as a pseudo-gate, exhibits an operating "gate" current much like the JFET, which is principally dependent on the drain-body voltage and to a lesser extent on drain current.

8.3.1 The Depletion-Mode MOSFET

The operating characteristics of the small-signal, depletion-mode MOSFET closely resemble those of the JFET. As the drain voltage rises with a fixed-gate bias, we first witness the so-called triode region, where the increasing current closely follows Ohm's law. This is operation below pinch-off, where V_{DS} is less than $V_{GS(off)}$. As we continue to increase the drain-source voltage (substrate tied to source), the conductance ($1/r_{DS(on)}$) gradually decreases and we see the drain current begin to saturate. Although this operation is reasonably similar to the JFET, there is sufficient dissimilarity to warrant our examination of the equations for drain current and transconductance.

For the depletion-mode MOSFET:

$$I_D = \frac{K}{2}(V_{GS} - V_{GS(off)})^2 \qquad (8.11)$$

$$g_{fs} = \frac{dI_D}{dV_{GS}} = K(V_{GS} - V_{GS(off)}) \qquad (8.12)$$

where V_{GS} exceeds $V_{GS(off)}$ and V_{DS} is greater than the difference.

8.3.2 The Enhancement-Mode MOSFET

We learned earlier that, operationally, the enhancement-mode MOSFET bears little resemblance to the small-signal JFET except that it too has a triode (Ohmic) region and a pentode (or saturation) region. At zero bias, whether the MOSFET is n-channel or p-channel, the MOSFET is OFF.

For the enhancement-mode MOSFET, the equations follow closely those of the depletion-mode MOSFET:

$$I_D = \frac{K}{2}(V_{GS} - V_{GS(th)}) \qquad (8.13)$$

$$g_{fs} = \frac{dI_D}{dV_{GS}} = K(V_{GS} - V_{GS(th)}) \qquad (8.14)$$

where V_{GS} exceeds the threshold voltage, and V_{DS} is much greater than the difference.

Biasing the enhancement-mode MOSFET to initiate drain current requires raising the gate voltage (same polarity as the drain) above the threshold voltage V_T. Since the more common use of enhancement-mode MOSFETs is in logic (or switching) applications, the principal goal in establishing the correct bias is to maintain compatibility with various forms of logic. When logic 0 (low) is at zero volts, we fix the gate bias at zero to ensure that the MOSFET is OFF. When the logic state is 1 (high), the MOSFET is ON, provided, of course, that the gate voltage rises sufficiently above threshold to establish turn-ON.

Problems may arise when we attempt to combine a *discrete* n-channel MOSFET and a p-channel enhancement-mode MOSFET to simulate a CMOS structure. More often than not the devices may have mismatched thresholds (V_T), which may result in shoot-through currents during switching. This shoot-through is minimized if we maintain rapid switching. Standby power dissipation is negligible when MOSFETs are used in the CMOS

configuration, whereas during switching such dissipation becomes a function of the shoot-through current and the switching speed.

8.4 Powering Up the Large-Signal (Power) FETs

Unlike our experience in powering up small-signal FETs and MOSFETs, when we operate large-signal FETs we may be handling substantial power, if not also high voltages. Remember that metal packages, such as the popular TO-204 (formerly the TO-3), have the drain tied to the case, thereby maintaining the case at the operating drain voltage. Likewise the plastic-packaged transistors have drains common with their metal tie-down tabs. *Potential lethal voltages may be on either the case or the tab.*

One precaution that needs continual emphasis: take special care to remember that *all* FETs—and in particular power FETs—operate through the application of a gate-to-*source* voltage. If you use an n-channel FET where the load is between source and ground and you drive the gate with a potential referenced to ground, you may be in for a rude awakening. Study Figure 8.10 to understand the problem.

8.4.1 The Static-Induction Transistor

Although not universally popular, the SIT may find application both as an amplifier and as a switch. As an amplifier it resembles the triode and, for the most part, we can follow the design procedures for the triode vacuum tube to develop suitable SIT circuits. Consequently, for either amplifier or oscillator service, if we have the output characteristics for the SIT (see Figure 2.7), using the graphical analysis routine, we begin with a suitable load line superimposed on the output characteristics (see Figure 4.14).

The simplest amplifier circuit, shown in Figure 8.11, yields the relation:

$$e_d = V_{DD} - i_d R_L \qquad (8.15)$$

The line, repeated in Figure 8.12, passing through the following points:

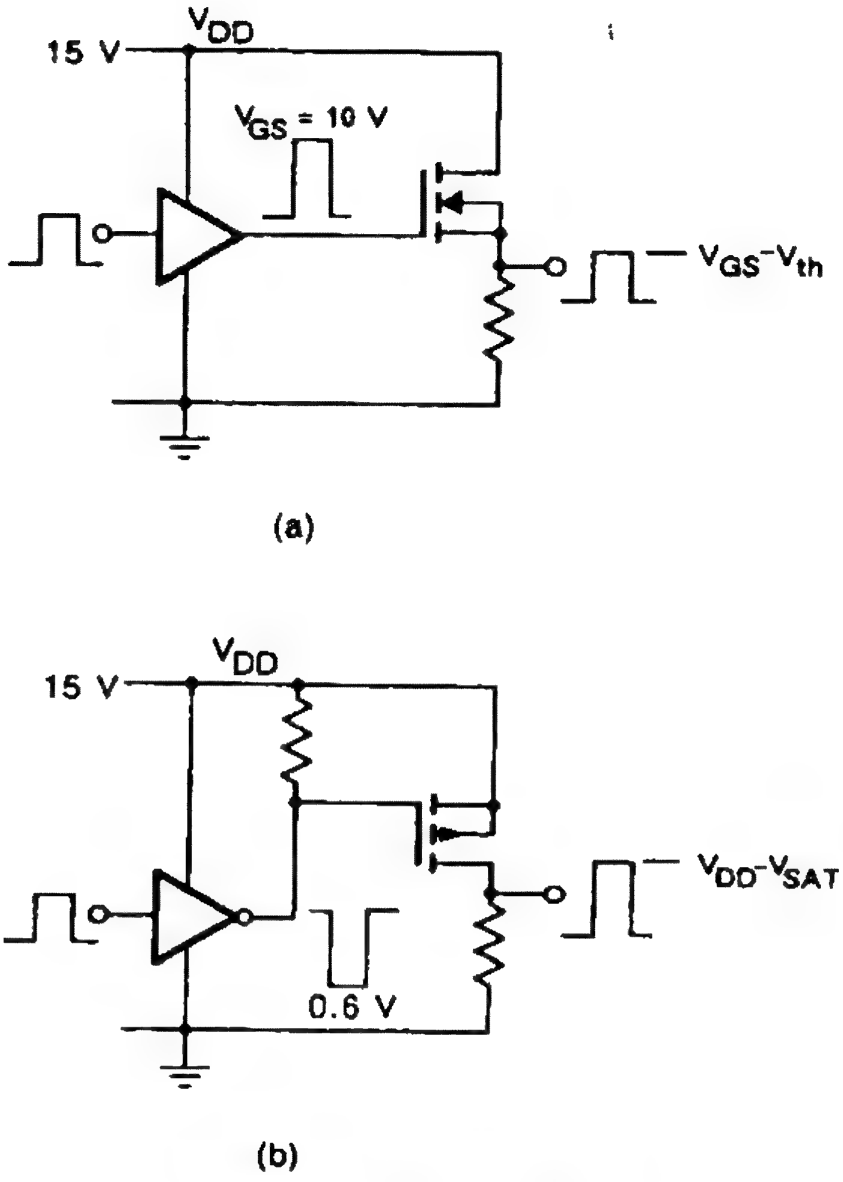


Figure 8.10 (a) Because gate drive is *always* referenced to the source, the n-channel, enhancement-mode MOSFET performs poorly as a source follower (series-connected switch). The output voltage is limited to $V_{GS} - V_{th}$. (b) The successful series-connected switch uses a p-channel, enhancement-mode MOSFET with gate referenced to $+V_{DD}$ (OFF) and pulled down to turn ON.

$$i_d = 0 \qquad V_d = V_{DD}$$

$$i_d = \frac{V_{DD}}{R_L} \qquad V_d = 0$$

is called a *load line*. With a value of R_L at the established operating voltage V_{DD}, at the bias level selected (the "Q" point in Figure 8.12), we may determine the operating drain current I_D.

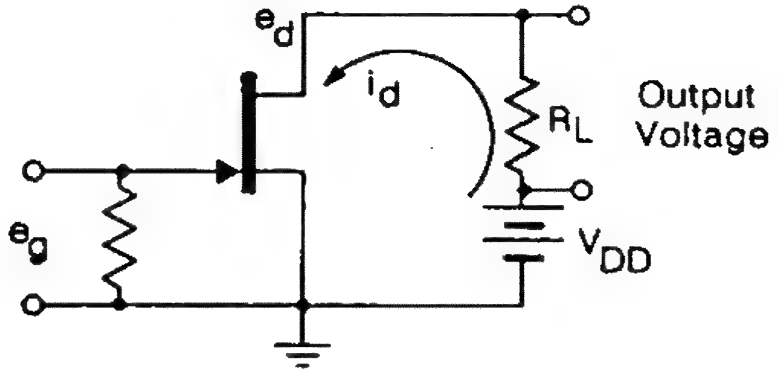


Figure 8.11 A simple Class A FET amplifier circuit.

The practice of using the depletion-mode SIT as a switch, is, in principle, similar to using the JFET, except that with the SIT, $V_{GS(off)}$ and the input capacitances are generally much larger, requiring both higher cutoff voltages and heavier drive current (see Eq. 3.9).

8.4.2 The Power DMOSFET

This popular power FET is finding use in a variety of switching applications as well as in amplifier service. Its near-linear trans-

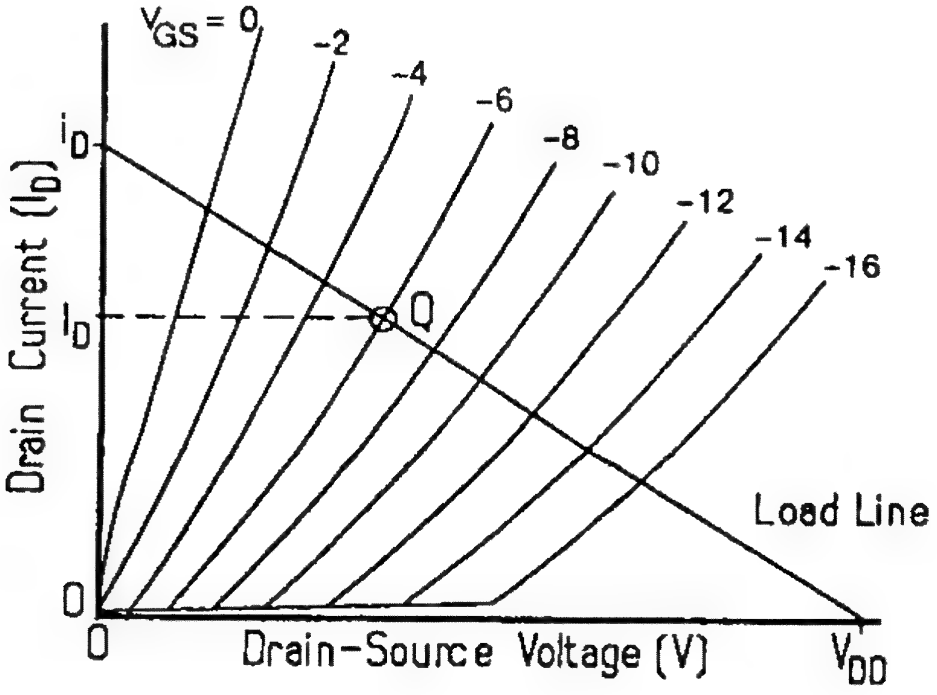


Figure 8.12 Load line and "Q" point of the simple Class A amplifier. Fixing a bias level establishes the operating drain current.

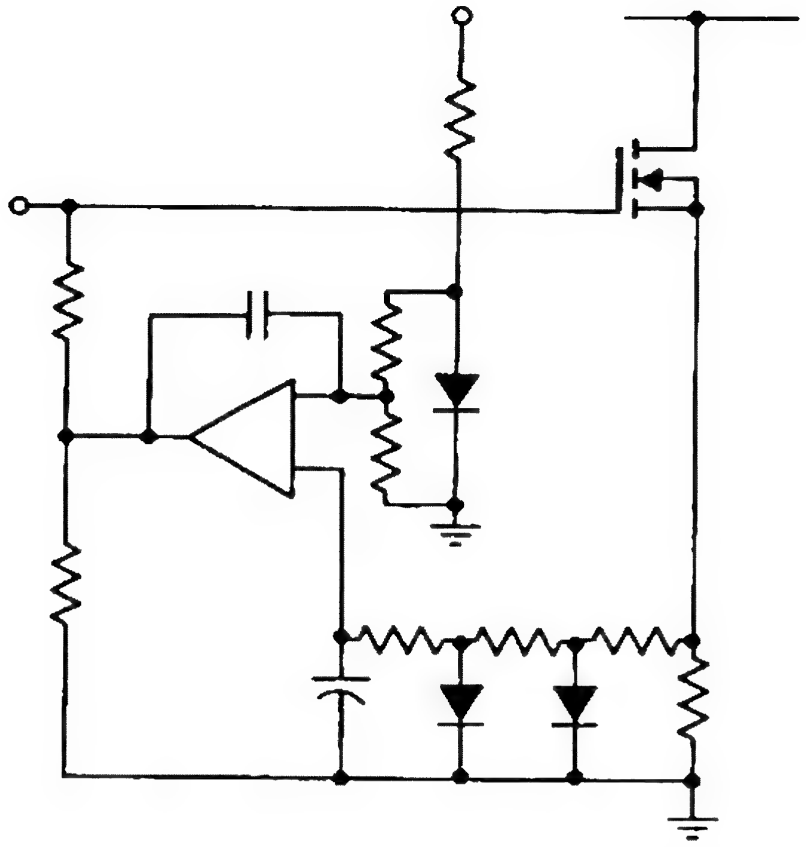


Figure 8.13 An op-amp helps in establishing the quiescent operating drain current of an enhancement-mode power DMOSFET audio amplifier. (From W. D. Roehr, "A Simple Direct-Coupled Power MOSFET Audio Amplifier Topology Featuring Bias Stabilization." Copyright © 1982, IEEE. Reprinted with permission from *International Conference on Consumer Electronics*, June 9–11, 1982, pp. 136–7.)

fer characteristic in the velocity-saturated region (see Figure 4.27) accounts for the popularity of the transistor in amplifier work.

When using the power DMOSFET in audio amplifier applications, because of the threshold voltage and its dependence on temperature (~ −6 mV/°C)—and perhaps a more insidious dependency on factory lot-to-lot variances—biasing the DMOSFET often requires some form of feedback to maintain the quiescent idle drain current. The op-amp generally finds service for this task, as shown in Figure 8.13.

Biasing the power DMOSFET for switching is easier because our sole concern is with either a full ON or a full OFF condition. To adequately understand and cope with the biasing necessary, we need to remember that the DMOSFET, like *all* FETs and bipolar transistors, is a *charge-coupled* device. Aside from bear-

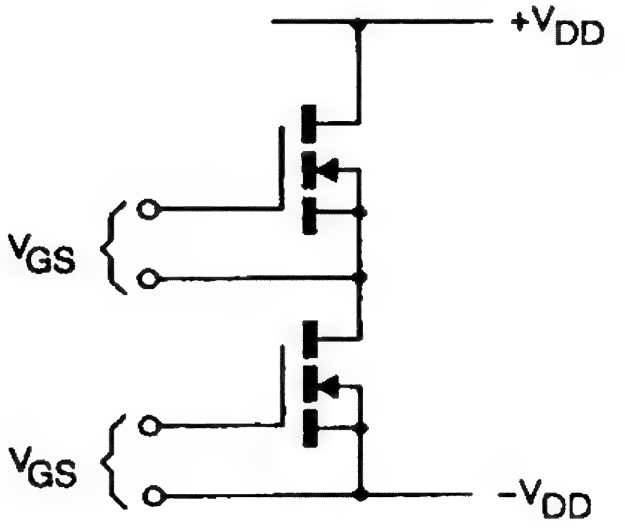


Figure 8.14 Biasing is *always* referenced to the source of the FET in question, irrespective of location within the circuit.

ing in mind that the FET exhibits no storage time and, therefore, switches faster than its equivalent bipolar transistor, we need to be aware that our biasing will, to some extent, be responsible for the ultimate switching efficiency.

It is important to remember that any gate bias for *any* FET must be referred to its source. Our drive is always V_{GS}, never V_G alone, or to ground (unless, of course, the FET source is also at ground). This is especially critical when driving DMOSFETs in totem-pole configurations, such as in H-bridge motor drives, or in any cascade configuration where the upper DMOSFET has a fluctuating source reference, as illustrated in Figure 8.14.

When operating the power DMOSFET as a switch, we need to be cognizant of the data sheet specifications, especially the gate-to-source voltage necessary to achieve the lowest ON resistance ($r_{DS(on)}$: Figure 7.12). If we bias the DMOSFET only to achieve our desired operating current, without taking due precautions of $r_{DS(on)}$, we may have an excessively high V_{SAT} (Figure 7.14), and we may exceed the dissipation of the transistor. When using the power DMOSFET as a switch, it is best to switch it fully ON (and OFF)—and switch it *fast*.

Aside from applying the necessary gate bias voltage to achieve sufficient drain current (or, preferably, lowest $r_{DS(on)}$), we must be sure to supply sufficient drive current to overcome the effects of capacitance. Any trapezoidal gate drive, or otherwise slow turn-ON gate drive, will only tend to cause excessive power dissipation in the DMOSFET and should be avoided, if possible.

Switching the power DMOSFET at speeds equaling or exceeding the data sheet specifications can, at times, be frustrating if we are not prepared to deal with the effective input capacity. Remember we are *not* dealing with C_{GS} alone, but with the greater contribution called the Miller capacitance, which, together with C_{gs}, may be a formidable load for any logic driver. It takes more than +10 V to switch an n-channel DMOSFET, it often takes power. *All* FETs (whether n- or p-channel) are charge-coupled transistors; they differ from bipolar transistors in that once turned either ON or OFF, they no longer require sustained drive. Initially, in the turn-ON or turn-OFF cycle, you may see little difference in the drive requirements between FETs and bipolar transistors.

To gain a better appreciation of the drive current the following equation is useful:

$$i = \frac{C\ dV}{dt} \tag{8.16}$$

where

C = total effective input capacity
dV = change in gate drive voltage
dt = speed you wish the FET to switch

Although driving from ±15 V CMOS is desirable, to overcome the Miller effect of the larger power DMOSFET, it often is advisable to use intermediate stages of smaller capacity DMOSFETs arranged in the classic CMOS totem pole. The classic CMOS stage is an inverter; that is, a positive-going input pulse results in a negative-going output pulse. If we wish to drive a large n-channel DMOSFET, our initial driving pulse to the power CMOS driver must be negative-going, as seen in Figure 8.15.

8.5 Powering Up the Insulated-Gate Bipolar Transistor

The IGBT will have application only as a high-current, high-voltage switch. Turning it ON or OFF is not unlike what we have just described for the power DMOSFET, but with one exception: we must not crowbar the gate (short the gate to emitter) to achieve a faster turn-OFF. The IGBT has what might

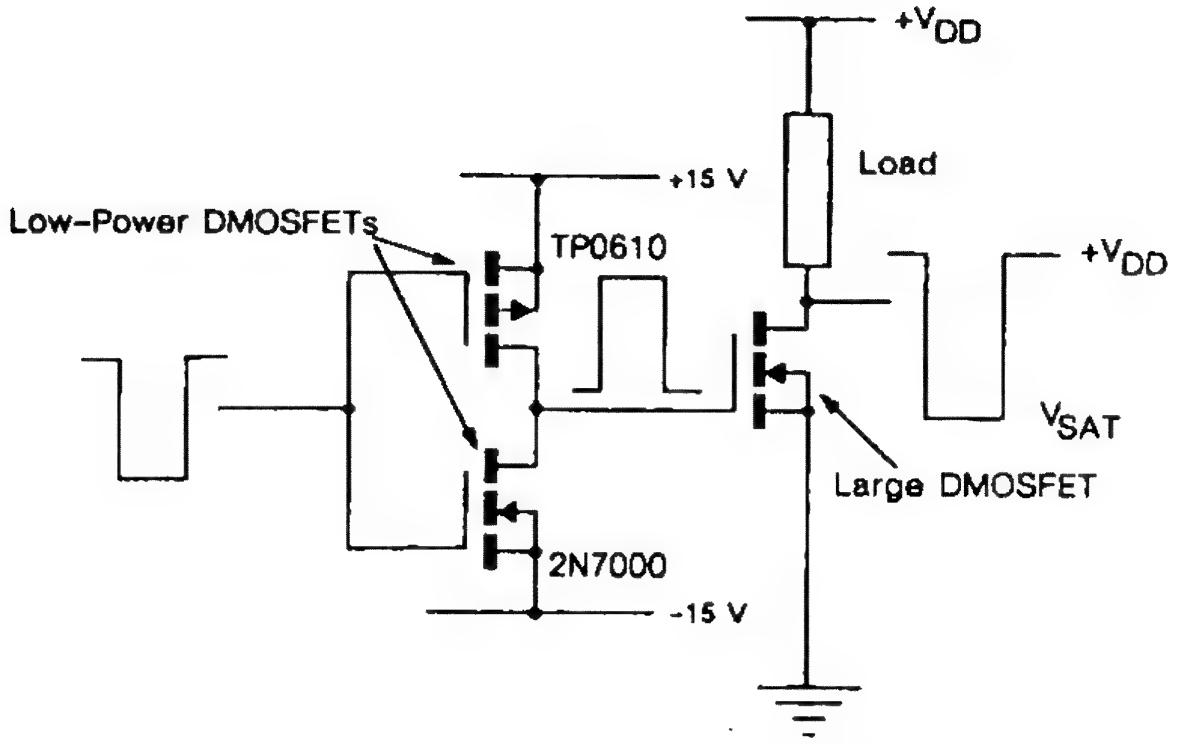


Figure 8.15 To achieve a high-current drive, use a pair of low-power-rated, n- and p-channel, enhancement-mode power MOSFETs to drive the large MOSFET. Note that the CMOS totem pole inverts the drive signal.

be called a maximum *controllable* collector current that depends on the turn-OFF slew rate of the gate. If, in an attempt to discharge the gate too swiftly, we lose control of the collector current, a runaway condition leading to latch-up may occur.

Like the power DMOSFET, the IGBT gate represents a capacitive impedance. Like all transistors, the IGBT is a charge-coupled transistor, and turn-ON becomes a function of how much current can be delivered (Eq. 8.16). Consequently, it is to our advantage to drive the IGBT gate from a low impedance. However, a low-drive impedance acts both to deliver more current to the gate and to accept more current from the gate. Conceivably, a low-gate-drive impedance might contribute to a loss of collector-current control. To thwart any mishap, Figure 8.16 offers a suggested gate drive circuit. Rapid discharge of the IGBT gate has little meaning because of the storage time that is inherent in the structure.

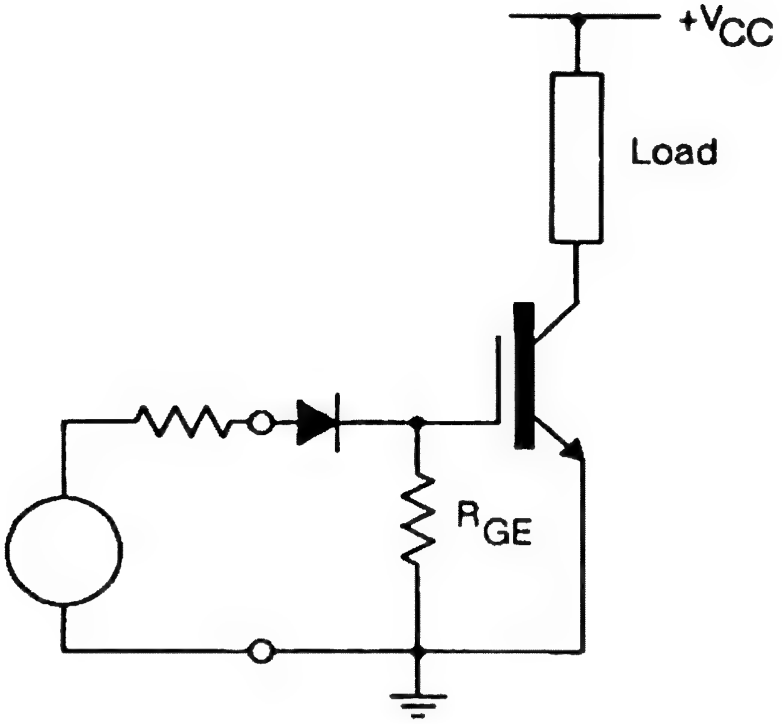


Figure 8.16 Driving the IGBT. The diode forces the gate to discharge through the gate-emitter resistor rather than through the low-impedance drive.

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9

Where Small-Signal FETs Are Found

9.1 Introduction

Despite the chapter title, we confess to giving the reader only a peek into the endless array of applications in which small-signal FETs are used. A basic building block, as the FET surely is, finds an astonishingly wide latitude of usage, ranging from toys to high-reliability military electronics—as well as everything in between.

Taking a broad-brush view, we can label the greater majority of applications as fitting into two general classifications: linear and switching. Let us further define analog as being a *linear* function and digital as being a *switching* function.

Confusion abounds when defining "small signal." We define it as dissipating less than 1 watt of d-c power.

9.2 FETs in Linear Circuits

JFETs and MOSFETs both find utility in linear applications but not necessarily in satisfying the same needs. The FET has distinctly unique characteristics not equaled by any other semiconductor. We remember Shockley's equation (Eq. 2.2), which identifies a square-law relationship between gate bias (V_{GS}) and drain current (I_D). This equation is a *power law equation*, which suggests that the FET, by definition, offers low distortion.

We can further substantiate this claim by examining the Taylor series power expansion, where we see the relationship of *signal* drain current i_d, to *signal* gate voltage e_g:

$$i_d = g_m e_g + \frac{1}{2}\frac{dg_m}{dV_G} e_g^2 + \frac{1}{3}\frac{d^2 g_m}{dV_G^2} e_g^3 + \cdots \qquad (9.1)$$

Linear Square law Cube law

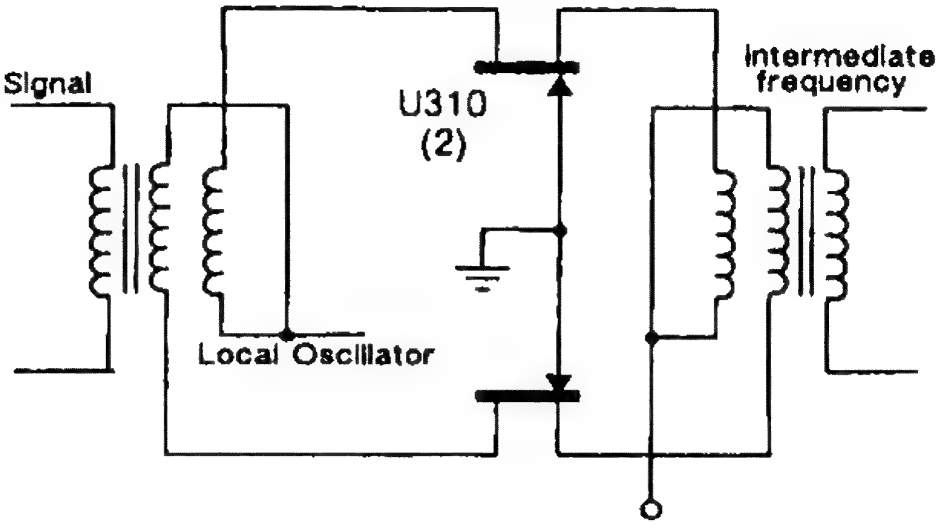
9.2.1 In Low-Distortion Applications

Since Shockley's equation identified the JFET as a *square-law* device, we can expect this Taylor expansion (Eq. 9.1) to decay rapidly after the second (square-law) term. The end result is that the JFET may perform as a *linear* (square-law) amplifier!

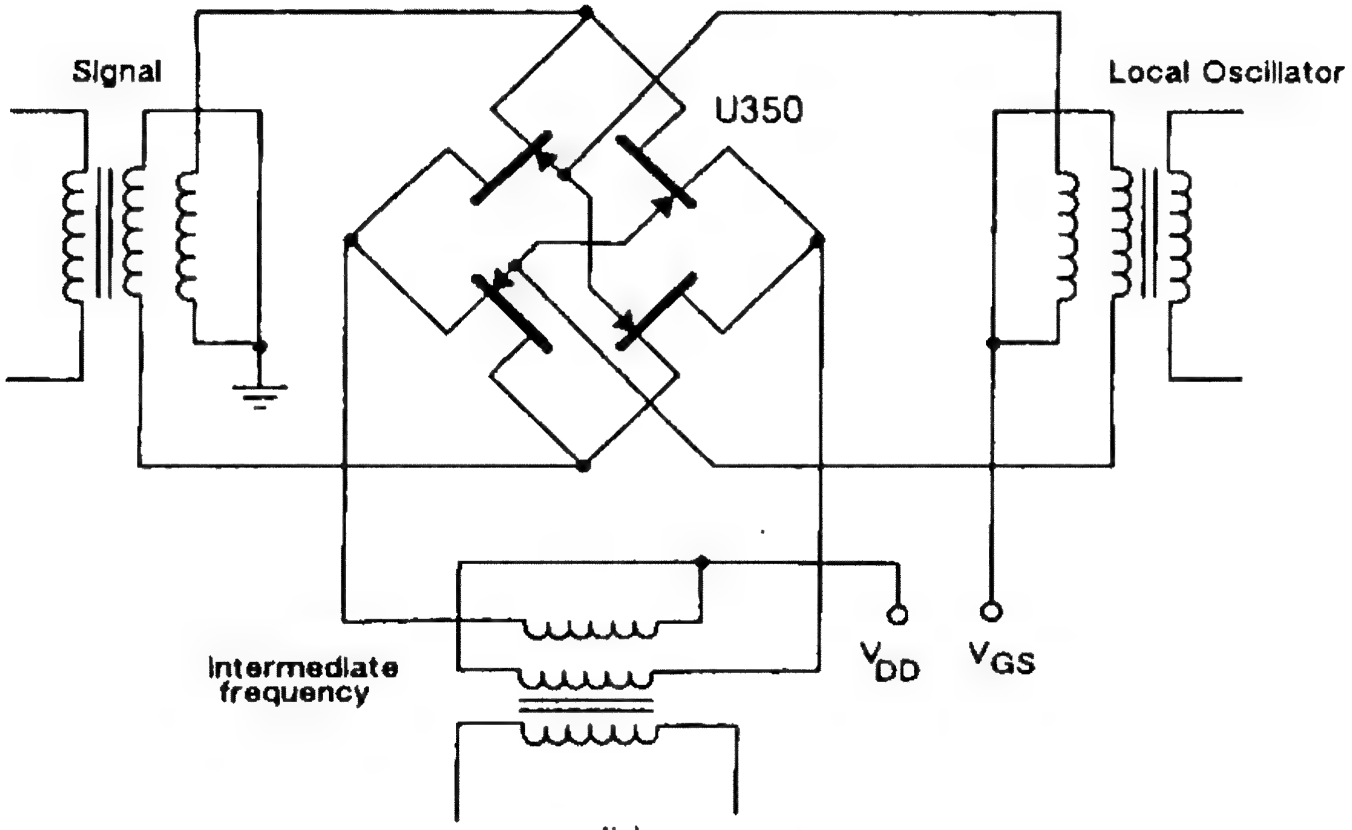
Not only does the small-signal FET perform as a linear element for amplifier service, but to further utilize its remarkable lack of higher order harmonics, as witnessed by Eq. 9.1, we also find the FET useful as a wide-dynamic-range, high-frequency mixer where square-law performance is crucial to end-use performance. Further reduction of harmonic distortion products may be achieved when the FET is used in either the single-balanced or the double-balanced mixer configuration, shown in Figure 9.1.

We must not be misled into believing that FETs are *perfect* square-law devices. Although Shockley's equation (Eqs. 2.2, 4.2, and 8.1) is often shown with the exponent of 2, such may not always be the case. Careful attention to the transfer characteristics of any FET or MOSFET will show highly nonlinear effects as we enter the conduction region. Unless we can avoid this region, we cannot avoid higher order responses. Despite this anomaly, the FET outperforms the bipolar transistor, whose transfer characteristics are exponential throughout!

Combining also the JFET's low gate current, low noise, and high input (gate) resistance with low parasitic capacitance and wide gain-bandwidth, we have an ideal transistor for both high-fidelity audio preamplifiers (Figure 9.2) and high-frequency radio-frequency amplifiers (Figure 9.3). Again, to ensure both a low gate current and a high input resistance, caution must be taken in the design phase to ensure that V_{DG} lies below the knee of the gate current curve (see Figure 4.8).



(a)



(b)

Figure 9.1 (a) Single-balanced JFET mixer for high-frequency operation. Intermodulation intercept point may reach beyond +30 dBm (input) with local oscillator drive levels of +17 dBm. (b) Double-balanced JFET mixer offers one-third less harmonic output than (a) due to the balance of both local oscillator and signal.

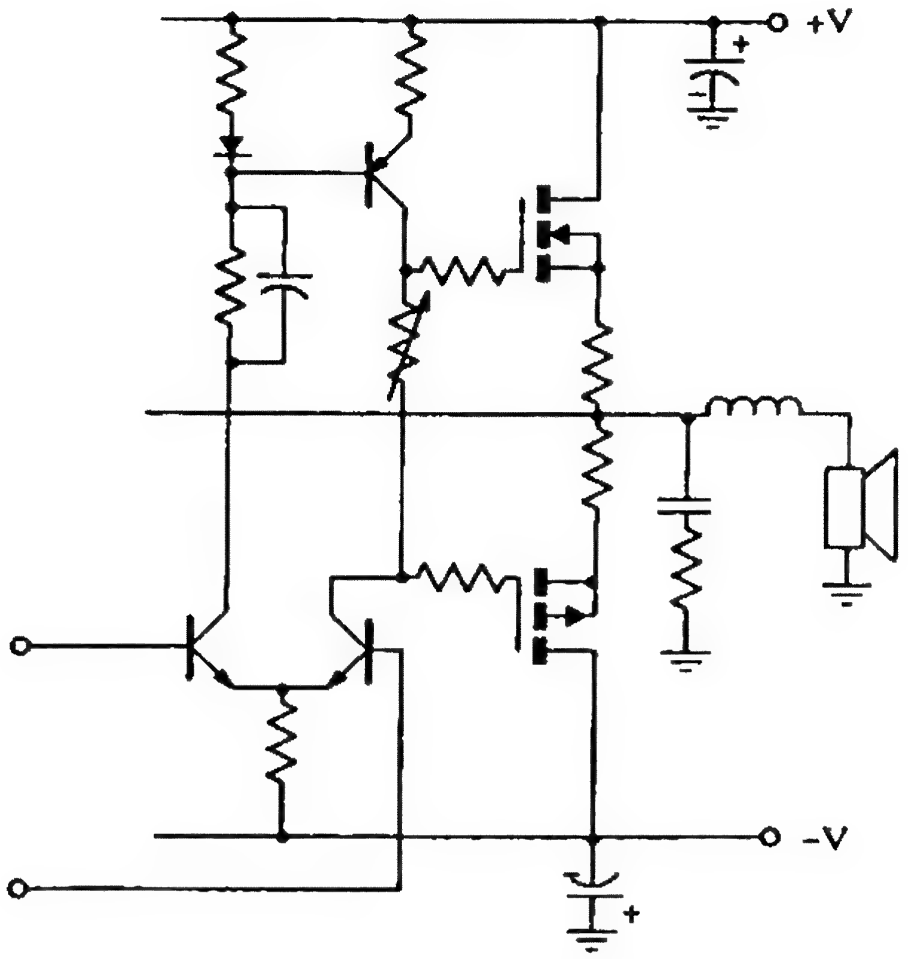


Figure 9.2 Using square-law FETs as push-pull (Class B) audio amplifiers greatly reduces the harmonic content and gives a pleasing audio effect.

9.2.2 In High-Frequency Amplifiers

When using the JFET in high-frequency applications, we have the option of using the transistor either in what is commonly identified as *common source* (as we saw in Figure 9.3) or in *common gate*, as seen in Figure 9.4. Both have their individual advantages and disadvantages. Summarizing these, the common-source amplifier with the high gate impedance provides higher gain. A major advantage is that the amplifier will provide a low noise figure simultaneously with high gain. A major disadvantage that offsets the high gain is the potential instability, which often requires critical neutralization (the inductive feedback circuit shown in Figure 9.3).

The common-gate amplifier offering a low input impedance makes matching easier and ensures stable performance without neutralization. Unfortunately, the lowest noise figure is not always accompanied by the highest gain.

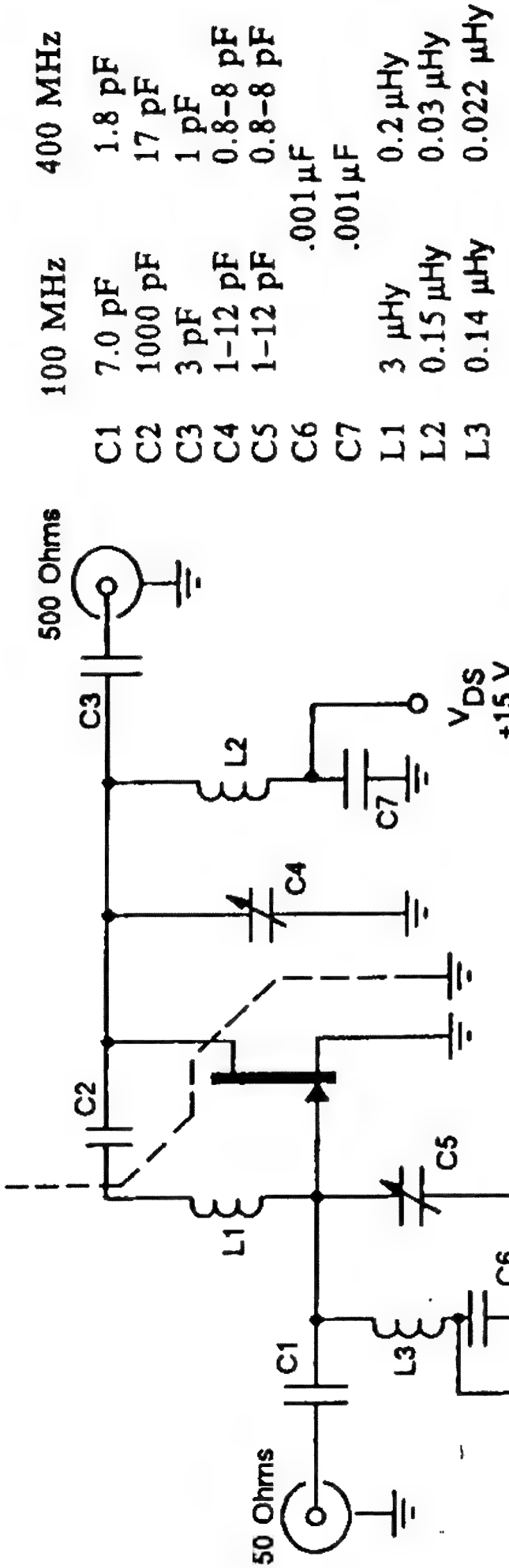


Figure 9.3 The JEDEC-registered, common-source amplifier circuit for the 2N4416. Note the inductive feedback necessary to establish stability.

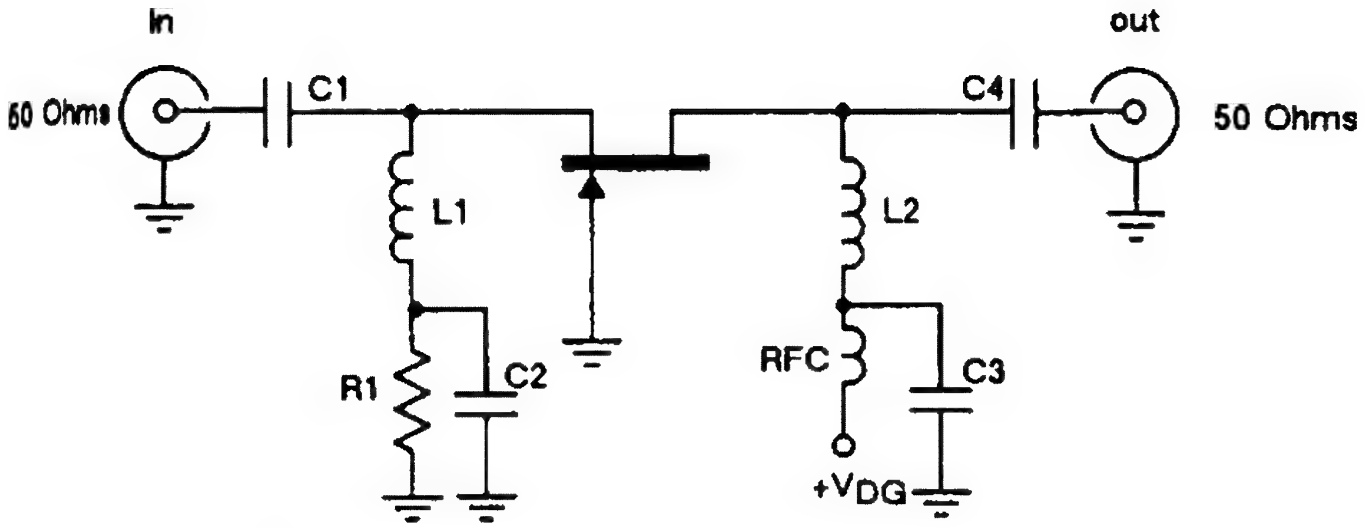


Figure 9.4 The typical common-gate amplifier offers stability under adverse load conditions.

When using FETs, we need to remember that because of their intrinsically high gate/drain impedance, FETs tend *not* to be broad band. Although common-gate operation will broaden the *input* circuit, the drain impedance remains high and the resulting overall bandwidth is narrow.

JFETs that have been popular in applications from high through ultrahigh frequencies are the 2N4416, used in the common-source configuration, and the U310 series, especially designed for use in common-gate circuits. These JFETs have been fully characterized for high-frequency service, and either admittance or S-parameter data may be found on their data sheets.

The once-popular dual-gate MOSFETs that used to be common in all TV tuners are, for the most part, built and supplied by offshore vendors. The dual-gate MOSFET, which is actually a cascade pair of MOSFETs, has an outstanding gain-bandwidth because of its phenomenally low feedback capacitance. Yet, its drain impedance is as high as that of the more common single-gate MOSFET.

9.2.3 As Video Amplifiers

JFETs perform remarkably well as video amplifiers offering gain-bandwidth products in excess of 200 MHz. Coupled with high d-c input (gate) resistances, low input capacitances, and flat group delay, they are aptly suited for the first stage of am-

plification in video cameras where low (1/f) noise is extremely important.

However, to achieve the desired bandwidth requires special attention to the input impedance match of the amplifier. Generally, the higher the impedance, the narrower the bandwidth. By referring to the FET's admittance parameters, we discover that the input *resistance* varies inversely with the square of the frequency, whereas the input *reactance* is inversely proportional to frequency.

Regardless of the circuit considered for the video amplifier (common source, source follower, cascade, etc.), the bandwidth is determined principally by the RC time constant of the input circuit.

A suitable JFET for video camera applications offering extremely low 1/f noise and an excellent gain-bandwidth product is the 2SK152.

9.2.4 In High-Frequency Probes

The JFET's high input (gate) resistance provides an opportunity for signal sampling without the disadvantage of loading the circuit under examination. However, to ensure a high input resistance we must keep gate current low (see Figure 4.8 and accompanying text). An especially good JFET for high-frequency signal sampling is the 2N4416A. Because of its low parasitic reactances, it offers little or no signal distortion—provided, of course, that we observe proper caution with regard to its operating gate current.

9.2.5 In Sample and Hold Circuits

A high gate resistance makes the FET especially suitable for sample and hold circuits, such as that shown in Figure 9.5. Most sample and hold circuits operate from relatively high impedances, which frees us to use FETs with low channel conductance, exhibiting low gate-drain and gate-source capacitances, hence having negligible charge-transfer characteristics. Furthermore, since FETs also exhibit no offset voltage, these advantages greatly enhance their suitability in sample and hold applications. For applications in which the source impedance is high (> 50 kΩ), the 2N4117A series JFET is especially suited.

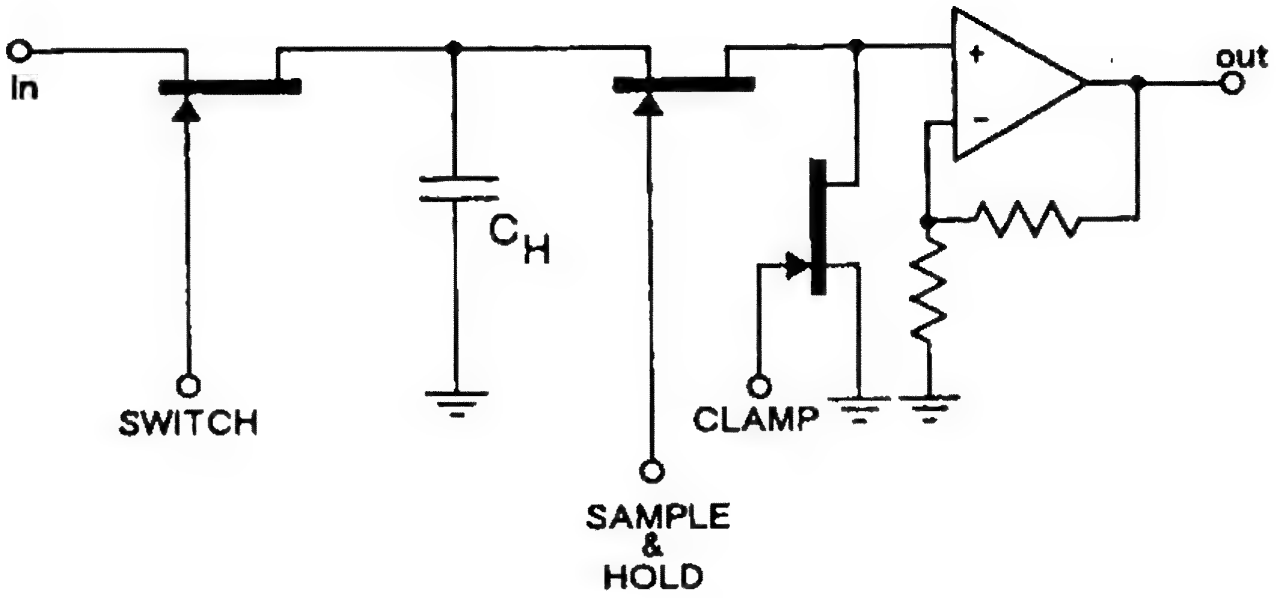


Figure 9.5 A sample and hold circuit using JFETs both for switching and sampling. The low gate-drain capacity reduces offset errors that might result from gate charge effects.

In one popular application, ion-detector smoke alarms, an ultrahigh gate-input resistance provides the sensitivity to ionized smoke particles necessary to trigger an alarm. The MOSFET commonly used is the p-channel, enhancement-mode 3N163, capable of sensitivities in the low femtoampere (10^{-15} A) range.

9.2.6 To Improve Op-Amp Performance

JFETs are often used to improve the performance of bipolar operational amplifiers (op-amp), shown in Figure 9.6. FET-input op-amps offer much lower input bias current with higher slew rates (20 V—40 V/μs is typical). Additionally, they provide a far superior frequency response because of reduced phase shift. Because of their close match of transconductance, the JFET-input op-amp exhibits dramatically improved CMRR. The JFET chosen for wide-bandwidth (to 100 MHz) service is the dual 2N5912. For lower frequency performance, the Siliconix U401 series is preferred because of its exceptional low gate current.

Improved performance can be achieved using cascade JFET duals, the principal advantage being a dramatic reduction in operating gate current due to the reduced drain-gate voltage on the input pair. An additional advantage of the cascade pair is

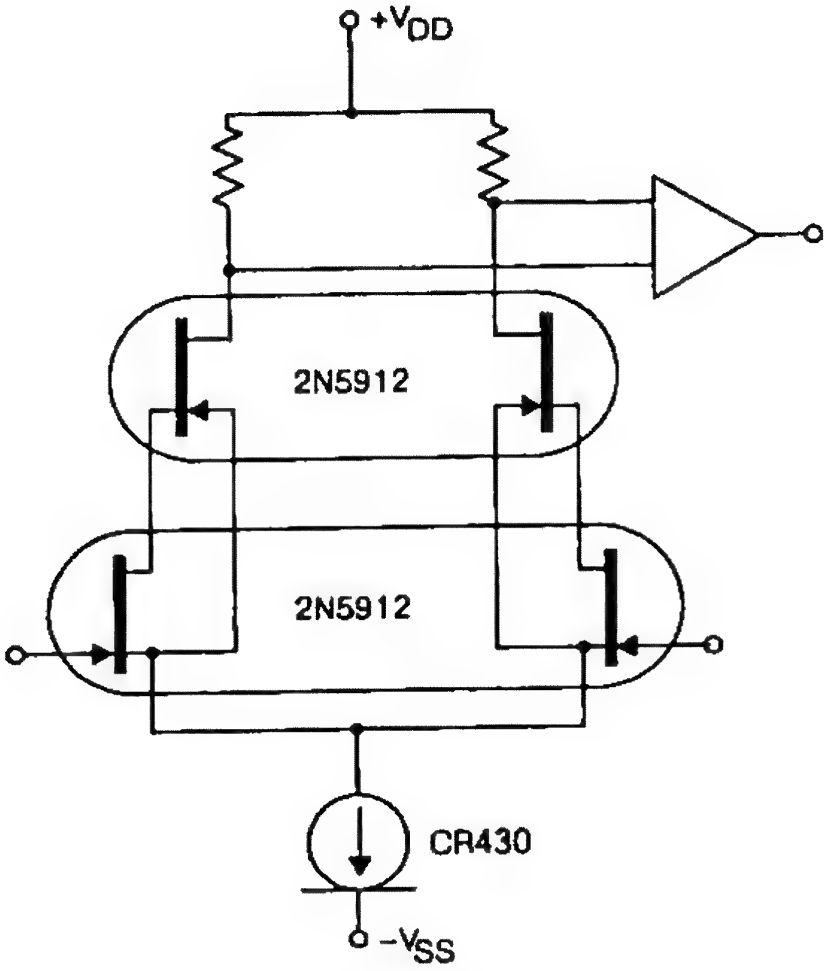


Figure 9.6 The cascade dual-JFET op-amp input ensures exceptionally low gate current and Miller capacitance. The gain-bandwidth of the 2N5912 can reach to 100 MHz. thus ensuring a fast slew-rate response.

a considerable reduction in Miller capacitance. As the Miller effect decreases, we see a progressively improved gain-bandwidth.

9.2.7 As Constant-Current Regulators

Because of the low output conductance of some JFETs, notably those with long gate diffusions (low-frequency devices), when operating in the saturation region they perform as current regulators over a wide voltage range (from just above V_p to slightly below $V_{(BR)DSS}$). The quality of current regulation is strongly dependent on the JFET's output conductance g_{os}, which, in turn, is closely related to its drain current. The output conductance decreases approximately linearly with I_D, be-

coming less as we bias the JFET closer to cutoff, $V_{GS(off)}$. Consequently, the lower the drain current, the better the regulation.

Alternatively, excellent regulation is achieved by using JFETs in cascade. Here the naturally low output conductance is further lowered by the degenerate feedback formed by the pair. The output conductance of the combination approximates the following:

$$\frac{g_{os}^{\,2}}{2g_{os} + g_{fs} + R_S\,(g_{fs}^{\,2} + g_{os}g_{fs} + g_{os}^{\,2})} \tag{9.2}$$

A JFET, either singly or in cascade, can be used effectively as a constant-current source by self-biasing the gate to establish the desired current (see Figure 9.7). The amount of bias is easily determined if we begin with Shockley's equation (Eq. 8.1) and solve for V_{GS}:

$$V_{GS} = V_{GS(off)}\left[1 - \left(\frac{I_D}{I_{DSS}}\right)^2\right] \tag{9.3}$$

Solving for the value of bias resistor, we find:

$$R = \frac{V_{GS}}{I_D} \tag{9.4}$$

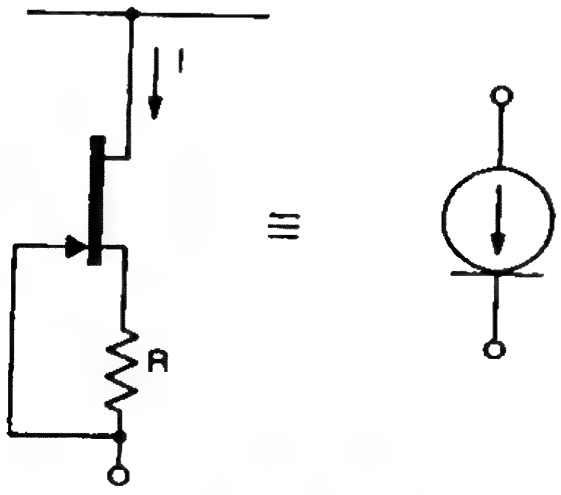


Figure 9.7 The JFET as a constant-current source and the symbol representing this.

JFETs exhibiting the desired long gate are easily spotted in the data sheet, where their low g_{os} gives them away. Such JFETs as the 2N4867 series find wide use as current limiters, as well as, of course, those that are specially designed for such service, such as the Siliconix CR and CRR series and the Motorola 1N5283 through 1N5314 series. Regulators offering higher currents with exceptional regulation can be constructed using the cascade arrangement with practically any JFET whose I_{DSS} is equal to or preferably greater than the current desired.

9.2.8 As Voltage-Controlled Resistors

A voltage-controlled resistor may be defined as a three-terminal device, as the JFET may also be defined. Under certain operating conditions ($V_{DS} << V_p$), the resistance between drain and source is a function of the gate-source voltage alone. However, there are restrictions in the use of uncompensated JFETs as VCRs. The fundamental restriction involves keeping the drain voltage low to ensure operation in the "triode region." A second restriction involves using the JFET as a VCR for analog signals, where third-quadrant performance is expected, as evidenced in Figure 9.8. Because of the nature of the gate-channel (pn) junction severe nonlinearity results once the drain voltage (the analog signal) has exceeded the barrier potential of the gate-channel junction (V_{bi}).

We may characterize the JFET as a VCR:

$$g_{os} = \frac{dI_D}{dV_{DS}} = \frac{-2I_{DSS}}{V_p(1 - V_{GS}/V_p)} \tag{9.5}$$

where g_{os} is, in reality, $1/r_{DS(on)}$.

To permit low-distortion performance of large analog signals, a simple feedback scheme (Figure 9.9) greatly reduces signal distortion.

9.2.9 In Cryogenic Amplifiers

Silicon carrier freezout is dependent to some extent on the doping concentration of the epitaxy, but generally little performance can be expected below 45 K for most JFETs. However, since the majority of cryogenic applications occur in liquid nitrogen

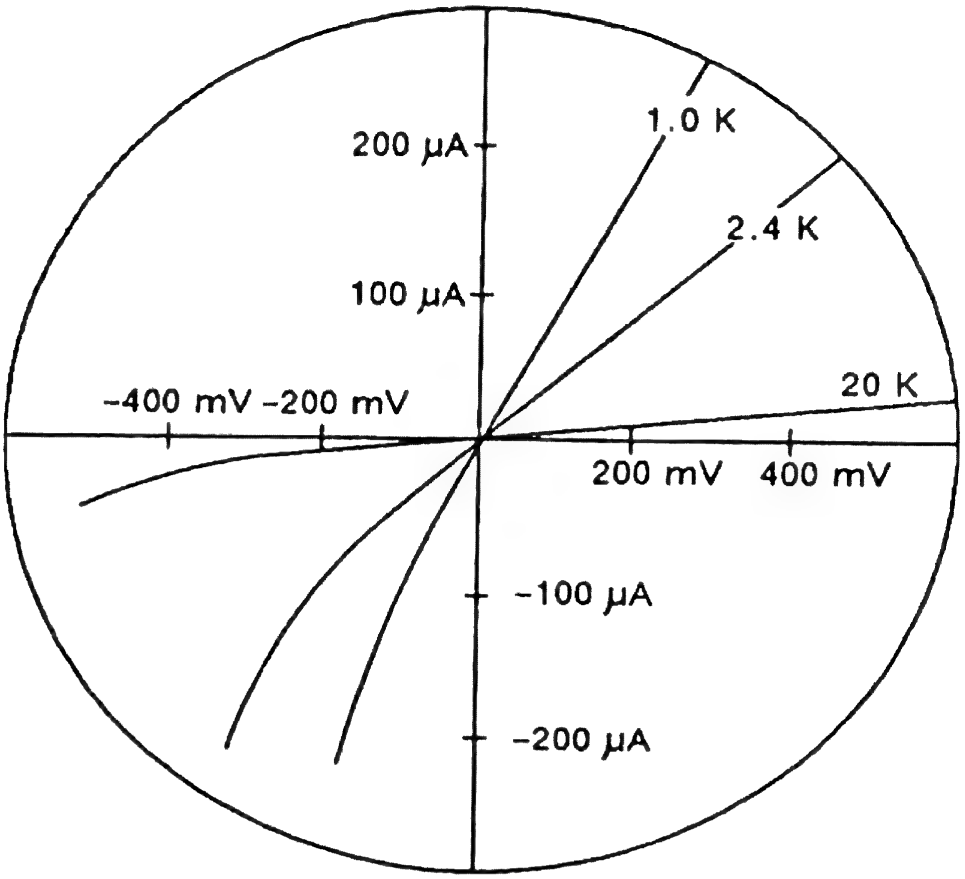
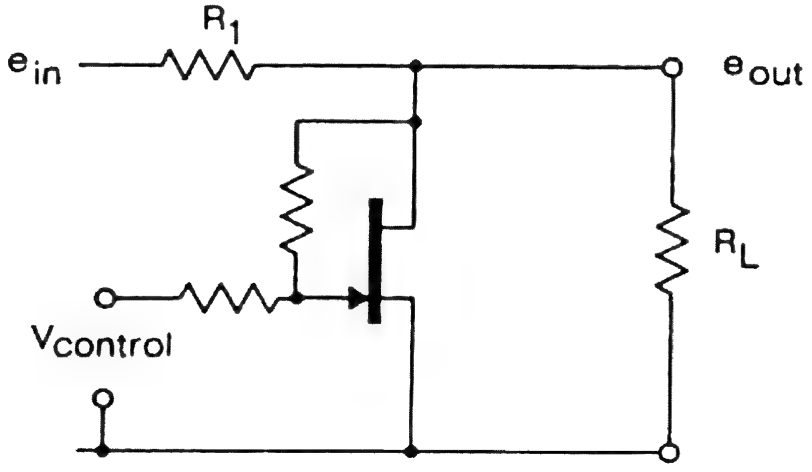


Figure 9.8 The JFET voltage-controlled resistor mimics the resistor in the first quadrant but runs into trouble if the third-quadrant signal voltage amplitude rises more than a few hundred millivolts.



$$e_{out} = e_{in} \frac{r_{DS(on)} \| R_L}{[r_{DS(on)} \| R_L] + R_1}$$

Figure 9.9 Third-quadrant compensation of the JFET VCR allows operation with analog signal voltages of considerable magnitude.

(77 K), the JFET is especially useful as a high-input-impedance amplifier because of its low gate leakage current and low flicker noise.

9.2.10 As Photosensitive Detectors

Although not readily available as a commercial product, the silicon JFET can be used as a photo-FET, combining in a single structure (the chip) both a photodiode—the gate structure—and a low-noise JFET amplifier structure. A truly efficient photo-FET needs a large surface area with an exposed gate thin enough to allow the light-created carriers to collect along the pn (gate/channel) junction. Commercial JFET chips do not provide optimum performance, although they have found application in sensing infrared radiation, where they appear to be most sensitive.

9.2.11 As Low-Leakage Diodes

We seldom appreciate the solution the JFET offers when seeking a low-leakage diode. The best diodes, capable of a minimum breakdown voltage of 34–40 V, will have reverse leakage currents ranging from 5 to 9 pA and up. Reflecting on what we have read in this volume, it comes as no surprise that the gate-to-channel p-n "diode" of the JFET offers remarkably low leakage at reasonable voltages. It is not a fast diode, but it does provide extraordinarily low leakages. Use the gate as the anode and either the drain or the source as the cathode. Clip the unwanted lead(s). Remember that leakage is dependent on both voltage and temperature (Eqs. 4.3 and 4.4).

9.3 FETs in Digital and Switching Circuits

Digital and switching applications have relied on FETs for many years. The many distinct advantages offered by FETs when used as switches have enhanced the popularity of these devices.

Although FETs offer a higher ON resistance than mechanical switches or relays, they have the advantage of providing a *consistent* ON resistance over the life of the switch. Naturally, if switching speed, and life, have any importance, the solid-state switch will always outshine the mechanical switch.

If our FET switch exhibits constant ON resistance as the signal amplitude varies, we then have no resistance modulation distortion. Distortion based on a varying resistance, $dr_{DS(on)}$, may be calculated as follows:

$$\% \text{ distortion} = \frac{100\ dr_{DS(on)}}{(R_G + R_L + r_{DS(on)} + dr_{DS(on)}} \qquad (9.6)$$

Yet, if our signal frequency is high enough to couple through the parasitic capacitances of the FET (C_{gd}, C_{gs}), it is conceivable that the resulting spurious gate bias might induce a form of resistance modulation! This would be progressively more serious as the signal frequency rose.

Comparing the FET switch to the bipolar transistor as a switch, we discover that FETs are bidirectional, offer higher OFF isolation, have no offset voltage, and, of particular importance, have *no minimum voltage* (aside from charge transfer, which, for low-level signals, may introduce "glitch" errors). Also FETs are much easier to drive.

OFF isolation for the FET depends on the performance and size of the isolation pn junctions. Consequently, the attenuation is dependent on both the impressed voltage across the junction and the junction temperature (see Eqs. 4.3 and 4.4). High-frequency OFF isolation is strongly dependent on the capacitance across the switching junction—usually drain-source capacitance—and is little affected by temperature.

Perhaps the most popular form of FET for digital applications is the complementary metal-oxide semiconductor field-effect transistor or CMOS, consisting of both an n-channel and p-channel MOSFET. CMOS transistors as well as discrete JFETs and MOSFETs have found wide application in switching both digital and analog signals.

9.3.1 In Logic Drives

Handling or receiving digital signals, such as from TTL, is generally not the task of the JFET because of its unpopular biasing requirements—needing two polarity rails—whereas TTL generally performs on a single (positive) polarity rail. However, the small-signal, n-channel, enhancement-mode MOSFET fits very well for both TTL and low-voltage CMOS (+5 V), since only one (positive) supply is needed. A MOSFET similar to the 2N7000

would perform quite well as a simple inverter in a TTL-driven application.

Emitter-coupled logic (ECL: also referred to as current-mode logic), unlike other popular forms of logic (CMOS and TTL), bases its superspeed on switching well-defined currents using nonsaturating bipolar transistors. The voltages involved in ECL are quite incompatible with FETs.

CMOS, in the traditional totem-pole circuit, finds extensive application as a high-current driver operating from balanced (±) rails, the p-channel enhancement "on top" tied to the positive rail, the n-channel enhancement underneath tied to the negative rail. Drains together make the output port.

Enhancement-mode MOSFETs offer distinct advantages in logic circuits. They are ideally suited to integration, where thousands of discrete circuits may be placed on a single silicon chip. Because of their threshold voltage (which maintains them normally OFF), they also offer good noise immunity. If integrated, the body is common to all and, to ensure optimum isolation, it is generally reverse biased.

MOSFETs find wide use in many areas. We can find them in transmission gates, inverters, bistable multivibrators, set/reset flip-flops, shift registers, and level shifters.

JFETs and MOSFETs find application in logic applications such as flip-flops, astable and bistable multivibrators, Schmitt triggers, level shifters, and inverters.

9.3.2 In Analog Switches

One of the earliest applications of both JFETs and MOSFETs was as the active switch element in integrated and hybrid analog switches and multiplexers. The JFET and the MOSFET have differing advantages and disadvantages. Whereas complementary MOSFET (CMOS) analog switches can handle analog signals "from rail to rail," the JFET switch is restricted by the need of maintaining sufficient negative bias to fully turn OFF the switch (see Chapter 8). Yet, if resistance distortion is critical, the JFET switch can outperform many CMOS analog switches.

Small-signal DMOS offers truly outstanding performance as a high-frequency analog switch. Not only can DMOS switch high-frequency signals but, unlike either the JFET or the classic MOSFET, it can switch them at very high speeds. Like the classic MOSFET, DMOS can be easily integrated into large single-chip arrays. An added benefit of DMOS that results from low

parasitic capacitance is its low charge injection—resulting from a combination of low gate-drain and gate-source capacitance—a phenomenon that, if left to chance, could introduce error into the signal channel.

Analog switches can be combined as multiplexers where several FETs, acting as switch elements, are joined to a common output. Again the type of FET will determine its performance, which is measured *not* by insertion loss, but, more commonly, by OFF isolation. Multiplexers, however, do have their share of problems. For example, drain capacitance is increased because of the paralleling of the active switch elements to a common output. An additional burden is *cross talk*—the superimposing of a spurious signal from an OFF channel on the desired signal. There are at least four causes for cross talk.

Leakage paths through finite OFF resistances
Capacitive coupling
Sampling
Radiated coupling

Only the last two need further discussion.

Sampling is easiest understood if we consider that the perfect multiswitch (multiplexer) should perform as *break-before-make*. Each switch element has to open before any of the remaining individual switches can close. Otherwise, we will have a short sample of the unwanted signal superimposed on the desired signal during that small interval when more than one switch is closed.

Radiated coupling occurs when the switch opens. The high impedance caused by the open, unterminated line develops a high-intensity electric field that may couple to adjacent switch elements or to adjacent transmission lines, shown in Figure 9.10.

Hybrid JFET analog switches are commercially available in a variety of switching configurations, such as SPST, SPDT, and DPDT, ranging upward from as low as 10 Ω. Switching speeds ranging from 150 to 250 ns are not the fault of the FET but of the inadequacy of the drivers. FETs switch as fast as you can charge and discharge the gate!

9.4 Combined in Hybrid Assemblies and Integrated Circuits

PMOS, NMOS, and CMOS are among the simplest of all FET integrated circuits. Early in the historical development of integrated

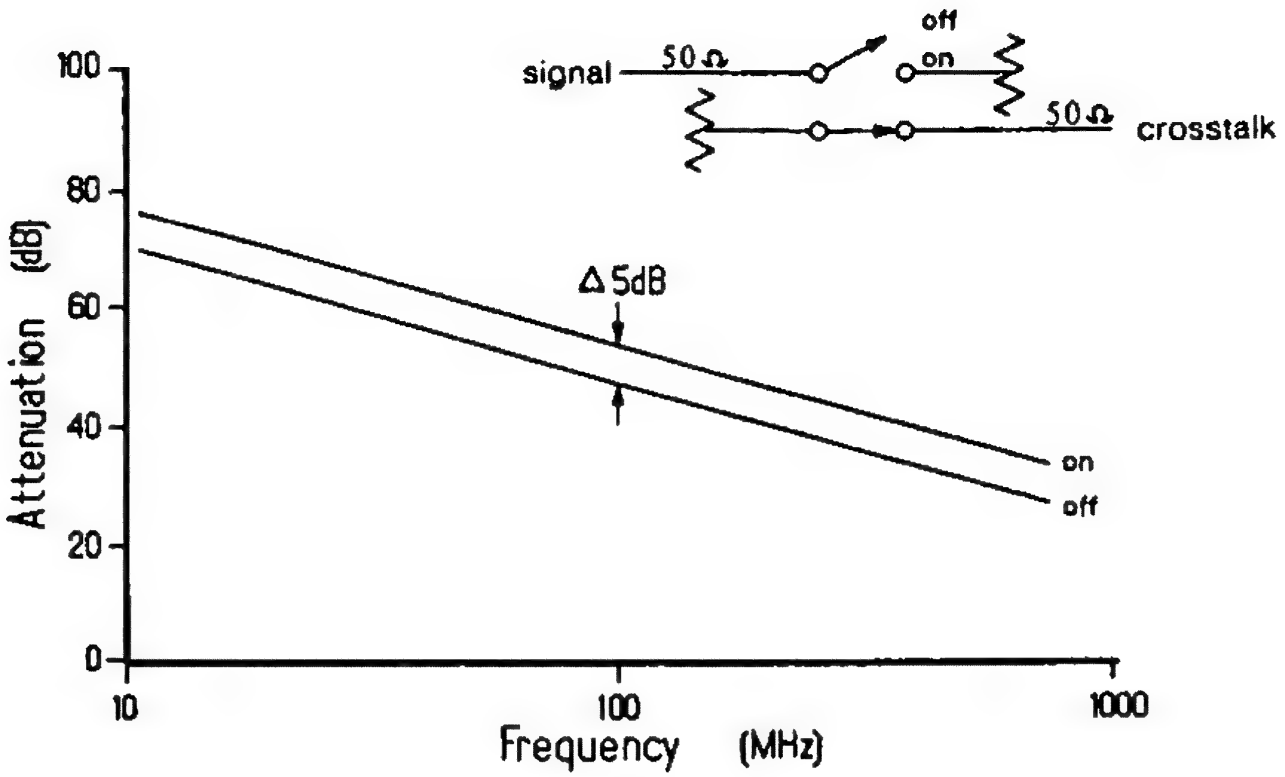


Figure 9.10 The effect of an open switch element of a double-pole, single-throw integrated circuit. The unterminated open end radiates to adjacent lines to effect a deterioration in cross-coupling by as much as 5 dB when compared to the cross-coupling of a closed switch (terminated).

circuits, PMOS (p-channel MOS) was popular, but it has been largely superseded by NMOS (n-channel MOS) and CMOS. JFETs have found some application in integrated circuits principally in FET-input operational amplifiers. The success of PMOS, NMOS, and CMOS is largely due to the ease in isolating functions. Whereas isolation diffusions are necessary with either the bipolar or JFET process, MOS calls for little or nothing in the way of isolating junctions. As a consequence, with the MOS process we see an extremely compact packing density, and the resulting chip has many functions.

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10

Where Large-Signal FETs Are Found

10.1 Introduction

Over the past dozen years during which the power DMOSFET has been gaining in popularity, we have been exposed to numerous applications, most of them involving using the FET as a switch. Many of these switching applications have been covered in other texts as well as in a variety of trade journals and symposium records. Because of the widespread acceptance of the power DMOSFET, we will, instead, explore somewhat novel applications that, to date, have received neither wide acceptance nor full appreciation. To be sure, some concepts described may need to be fully developed before they become practical. For others, we await the power FET needed to do the job.

The static-induction transistor, of Japanese invention, still seeks a market in the West. Although the device has great potential both as an amplifier and as a switch, the gate cutoff voltage, being of the opposite polarity from the drain, necessitates having two power supplies. Additionally, Western customers tend to buy only products that are available from multiple sources. Regretably, the Japanese vendors seldom offer identical part numbers for identical goods. Although they may, indeed, second-source a transistor, the unique part number assigned is mistakenly felt to represent a non-second-source item.

The insulated-gate bipolar transistor (IGBT) is still too new to have found wide application. We believe that if it is to become popular, a p-channel version will find wide application in

H-bridge motor drives, where, situated in the upper section, we will have greater flexibility without the constant concern of shoot-through currents and damaging dV/dt. However, because of its natural limitation due to storage time and current tailing, IGBT performance may be limited to switching applications under 50 kHz.

10.2 The FETlington

Many have compared the power DMOSFET with the Darlington pair because both exhibit a reasonably high input resistance and both offer high gain. But there the comparison stops. The bipolar Darlington has several shortcomings not evident in the power DMOSFET. Power bipolar transistors exhibit *storage time*—a debilitating slowness in turn-OFF. A pair of power bipolars—the configuration of a bipolar Darlington—only compounds the storage time problems. Then there is the problem of saturation voltage (V_{SAT}). For the bipolar Darlington V_{SAT} can be excessively high, especially when switching high currents. Then too, a bipolar transistor pair has the characteristic drive requirements. Although the input may seem high (as compared to a single bipolar transistor), we must continue to inject charge for as long as the Darlington remains conducting. Finally, we have thermal problems.

Yet, the power DMOSFET alone is *not* equivalent to the bipolar Darlington. We expect to see a tandem connection if we have a Darlington *pair*. Figure 10.1 shows such a tandem connection, an enhancement-mode, n-channel DMOSFET driving a power bipolar transistor, a *FETlington*.

The circuit has several variables that define the performance shown in Figure 10.2. The base-emitter resistance R_{BE}, coupled with the ON resistance of the DMOSFET (shown as R_{DS} in Figure 10.2), establish the base drive to the bipolar transistor. If we drive the bipolar transistor's base hard—a low R_{DS} and a high R_{BE}—turn OFF is characteristically slow because we have driven the bipolar device into saturation, where the V_{SAT} is exceptionally low.

Conversely, if we raise the R_{DS} of the circuit and lower R_{BE}, we reduce the drive current of the bipolar transistor's base. Being far from saturation, the bipolar transistor switches fast, but we pay with a high V_{SAT}.

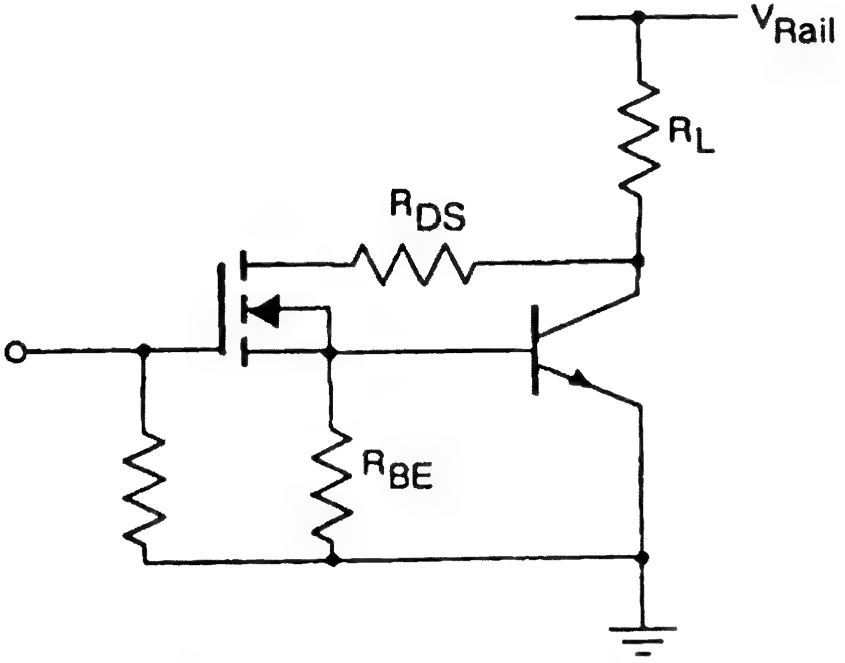

Figure 10.1 A "FETlington" consisting of an enhancement-mode DMOSFET driving a power bipolar transistor in cascade.

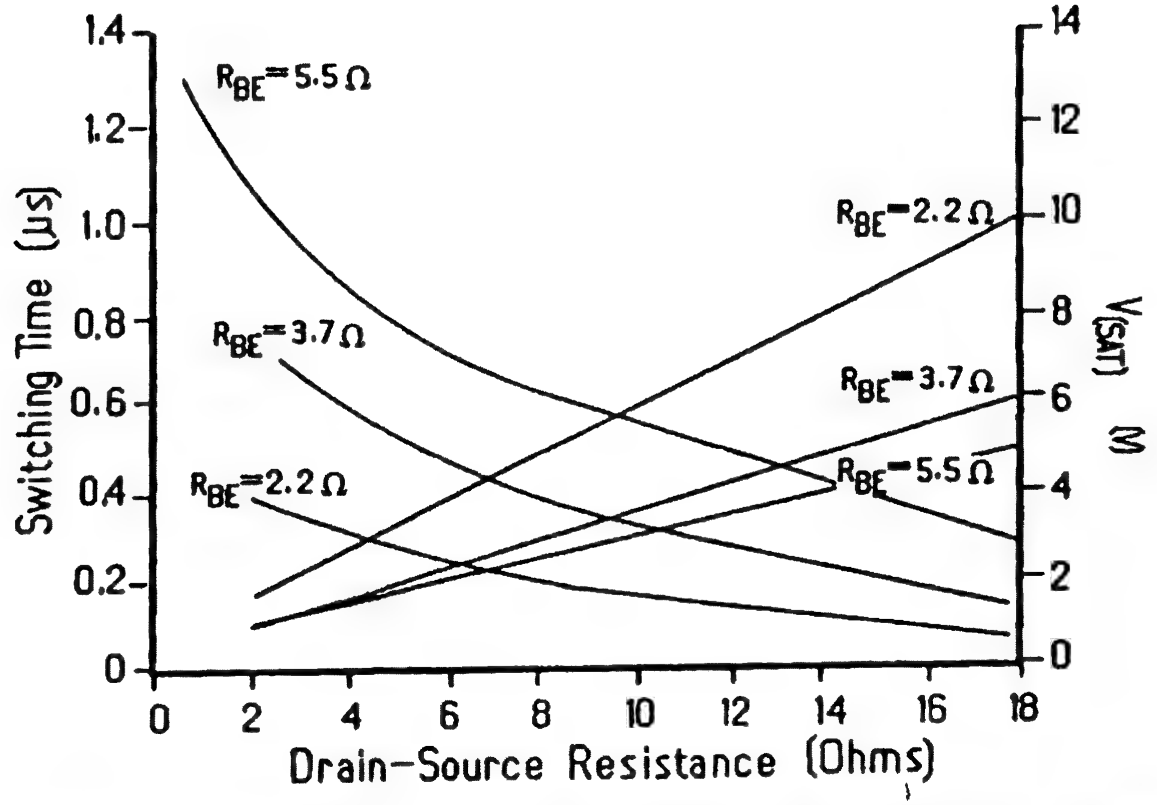

Figure 10.2 Switching performance and saturation characteristics of the FETlington are dependent upon base drive, which, in turn, is dependent upon R_{DS} and R_{BE}.

In this application both the DMOSFET and the bipolar transistor must be rated to withstand the full voltage.

The combination of a high V_{SAT} and a high collector current causes excessive heat buildup in the bipolar transistor. If adequate heatsinking is not available, thermal runaway may destroy the transistor.

A combination such as shown in Figure 10.1 might find use in high-voltage, high-current, applications, where if the power DMOSFET were used alone, its resistance would be a distinct disadvantage (see Figure 1.21). The power DMOSFET, acting alone, emulating the Darlington concept (a high gate resistance and high gain), would be no match for the FETlington in such applications.

The IGBT, with the MOSFET gate/bipolar transistor output, closely emulates the FETlington pair.

10.3 Paralleling the Power Bipolar Transistor and DMOSFET

Conceptually easy, paralleling the power bipolar transistor with a like-voltage-rated power DMOSFET, as shown in Figure 10.3, offers an opportunity to split the performance responsibilities between the two, using each to its advantage. The DMOSFET supplies fast switching; for power bipolar transistor, heavy current handling with a low V_{SAT}. The secret to success is in how we drive the pair.

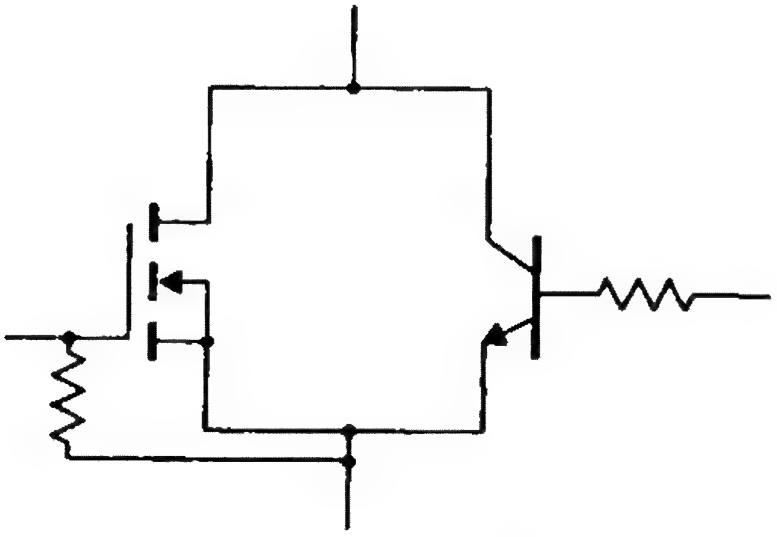

Figure 10.3 Parallel DMOSFET and power bipolar transistor splits performance responsibilities using each to its advantage.

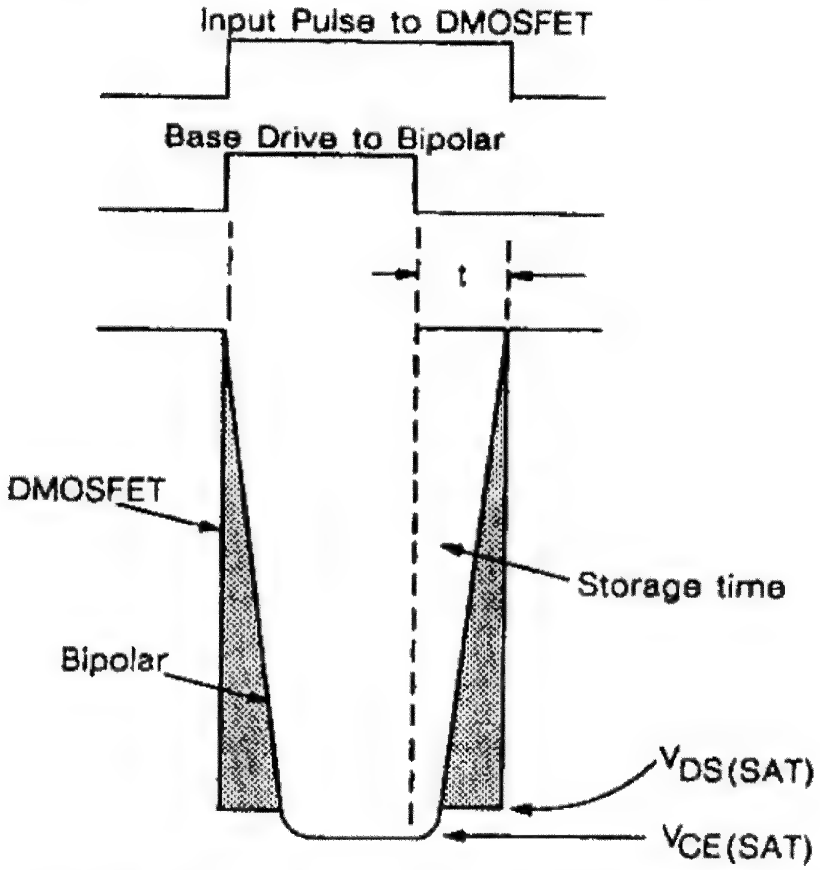

Figure 10.4 Resulting wave shape of the parallel DMOSFET/bipolar transistor. Note that the DMOSFET takes the brunt of the switching energy, especially during the storage-time delay (t) of the bipolar transistor, whereas the bipolar conducts the majority of the load current.

To drive the DMOSFET, we need a gate-source voltage sufficient for full turn-ON, perhaps +15 V for an n-channel. For the bipolar transistor, a current source sufficient to achieve saturation is necessary. Timing is critical, as we see from Figure 10.4. We drive both ON together; the DMOSFET will respond faster than the bipolar transistor. At the initial turn-ON, the DMOSFET takes the full load. Soon the bipolar transistor is into saturation, and with a V_{SAT} less than that of the DMOSFET, the work formerly carried by the DMOSFET transfers to the bipolar transistor. Turn-OFF is more complicated. The bipolar transistor must be deactivated first, followed by the DMOSFET, but not just at "any old time." We turn the DMOSFET OFF when the storage time of the bipolar transistor has subsided. Properly synchronized, the DMOSFET handles the load only while the bipolar transistor is turning ON and as the bipolar undergoes its slow turn-OFF. The resulting waveshape is shown in Figure 10.4. Although the IGBT can handle the cur-

rent, it exhibits the bipolar transistor's storage time, so the resulting waveshape can never be rectangular.

10.4 Emitter Switching with DMOSFETs

High-voltage, high-current power DMOSFETs are either nonexistent or expensive simply because, as we have seen, the $r_{DS(on)}$ rises faster than the breakdown voltage (see Eq. 4.5), thus mandating a large geometry to achieve a low ON resistance. As a potentially viable alternative, take a high-voltage power bipolar transistor suitable for withstanding the expected high voltage and a low-voltage, low $r_{DS(on)}$ power DMOSFET and connect them as shown in Figure 10.5. The DMOSFET performs as a simple switch. Note the advantages. The power DMOSFET operates with a low drain voltage—always less than the bipolar

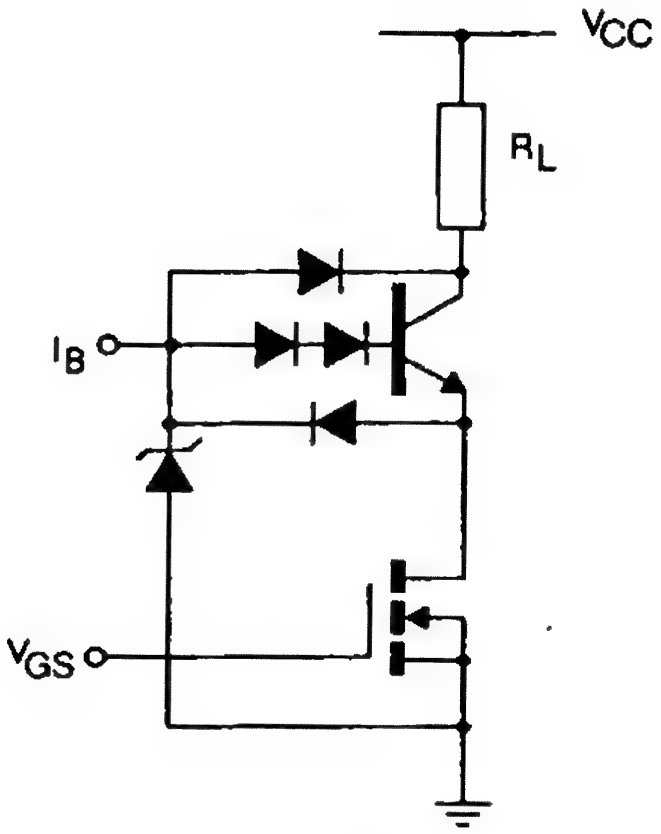

Figure 10.5 Cascading a DMOSFET with a power bipolar transistor. Commonly called Emitter Switching. To turn the combination ON, base current and a positive gate voltage must be maintained. Using a Baker clamp (the diode array on the bipolar's base connection) allows the bipolar to be used to its full V_{CBO} rating.

transistor's base voltage. As a consequence, the DMOSFET can have a very low $r_{DS(on)}$ as well as a low breakdown voltage specification and not be overly expensive. Even though the bipolar transistor may be driven into saturation (but in Figure 10.5 saturation is prohibited by the addition of a Baker clamp), once the DMOSFET has turned OFF, no emitter current can flow; the bipolar is OFF. What collector current was flowing is diverted into the bipolar's base and is shunted through the zener diode to ground. Both the storage time and any possibility of second breakdown are greatly reduced.

This combination can outperform any 1000 V DMOSFET as well as the IGBT, which is known for handling high voltages and high currents at low saturation levels (see Figure 1.21). Furthermore the emitter switcher can switch OFF more swiftly than an IGBT!

10.5 Power DMOSFETs as Synchronous Rectifiers

Because of an insatiable desire to maximize efficiency, we have seen the switch-mode power supply capture the power supply market. Power DMOSFETs, with their fast switching capability, not only have contributed to making this switch-mode power supply efficient but have contributed also to the switcher's near dominance in the market. Yet, for the greater part, within the workings of this same highly efficient power converter, the same pn junction rectifiers continue to waste power needlessly. Many low-voltage switchers have further improved their performance by replacing these pn junction rectifiers with Schottky barrier rectifiers; but for power supplies much above 75 V, because of the voltage limitation of the Schottky, the p-n diode rectifier remains.

As the manufacturing costs of ultralow-ON-resistance power DMOSFETs drop, we shall see even higher efficiency switch-mode power supplies using DMOSFET as *synchronous rectifiers.*

Power DMOSFETs are capable of passing current in either direction *provided* certain constraints are taken into consideration. The principal constraint is that the parasitic drain-source diode (Figure 4.6b) must remain OFF. That simply means that the IR drop ($I_D R_{DS(on)}$) *must* be less than the barrier potential of the parasitic diode (approximately 0.55 V at 25°C).

Although we have power DMOSFETs with data sheet values for $r_{DS(on)}$ approaching but a few milliohms, we must remember that as the chip temperature rises, so does the resistance. The higher the breakdown voltage, the greater the effect (Figure 5.15). Furthermore, as the temperature rises, the p-n diode barrier potential decreases! In other words, as the temperature rises, the advantages of the power DMOSFET and the disadvantages of the p-n diode converge! Conversely, as the temperature drops, the advantage of using power DMOSFET becomes more apparent, not only because the diode's barrier potential is rising but because the power DMOSFET's ON resistance is dropping, forcing the V_{SAT} (The voltage "across" the parasitic diode) down. Furthermore, we need to be reminded that the p-n diode under discussion is not only the rectifier we seek to replace but is also the parasitic diode that exists in the power DMOSFET!

Our problem with diode rectifiers is the *power* lost in rectification, $I_{rms}V_{bi}$. If we are pulling 10 A from our switcher and the diodes drop 0.55 V, our loss is 5.5 W! The power DMOSFET also has power loss, $I_{rms}{}^2r_{DS(on)}$, and if our ON resistance is 0.018 Ω, this loss equates to 1.8 W. Looking at these losses from a slightly different (and simplistic) perspective, we might have a power supply outputting 3 V. If the diode drop is a nominal 0.55 V, we would need a supply capable of delivering 3.55 V to the rectifiers. Rather poor efficiency! Using the DMOSFET, with an $r_{DS(on)}$ of 0.018 Ω, our drop would be only 0.18 V!

We need to find out when it pays to use power DMOSFETs as synchronous rectifiers in lieu of either p-n or Schottky barrier diodes. Many questions are involved: What output current do we need? Can we afford the low $r_{DS(on)}$ power DMOSFETs needed to handle this current? What is our operating temperature (and transistor junction temperature)? Are we willing to add the complex DMOSFET gate-driving circuitry to our already complex switch-mode power supply?

We can gain a better perspective of how performance determines choice by examining Figure 10.6, where, for an unrealistic operating junction temperature of 25°C (for both the Schottky barrier diode and the power DMOSFET), the graph indicates the more suitable rectifier. Clearly, the DMOSFET limit is a function of the bulk resistance of the epitaxy that also determines its breakdown voltage characteristic (Eq. 4.5). For silicon, the bulk resistance/breakdown voltage barrier is shown in Figure 10.7.

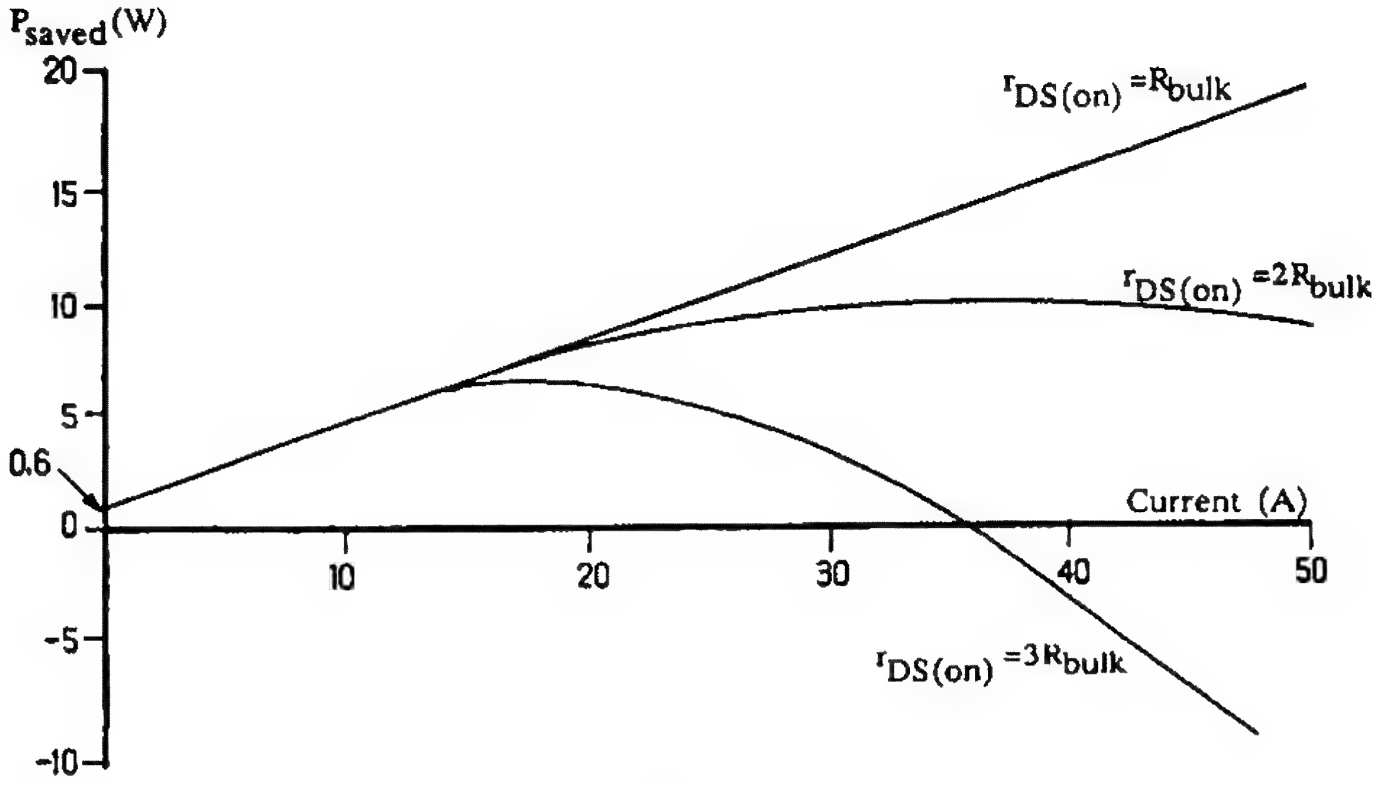

Figure 10.6 Comparing the efficiency between the Schottky barrier diode and the power DMOSFET (only for T_j = 25°C). If P_{saved} is positive, the DMOSFET is the preferred device; if P_{saved} is negative, the Schottky diode is the preferred device.

Aside from the power savings claimed from using power DMOSFETs as synchronous rectifiers, we must address the concept of *synchronicity*. To achieve the equivalent of rectification without using rectifiers requires some rather exotic gate drive.

Power DMOSFETs conduct equally well *in either direction*: in the normal direction, when the gate bias enhances a channel; in the reverse direction, through the parasitic diode that bridges the DMOSFET or, if the gate bias remains, through the enhanced channel—provided the V_{SAT} is *less* than the V_{bi} of this parasitic diode. It is by the latter means that we address the synchronous rectifier; we tied the *sources* of our n-channel, enhancement-mode DMOSFETs to the raw a-c, and from the drains we proceed to filter the "rectified" d-c, as we see in Figure 10.8. Gate drive must act in synchronism with the positive-going wave of the raw a-c impressed on the DMOSFET sources. If we miss synchronism, the parasitic diode becomes the rectifier and any advantage gained by using DMOSFETs vanishes. This needed synchronism may be more readily available in a switch-mode power supply than in the more conventional linear supply.

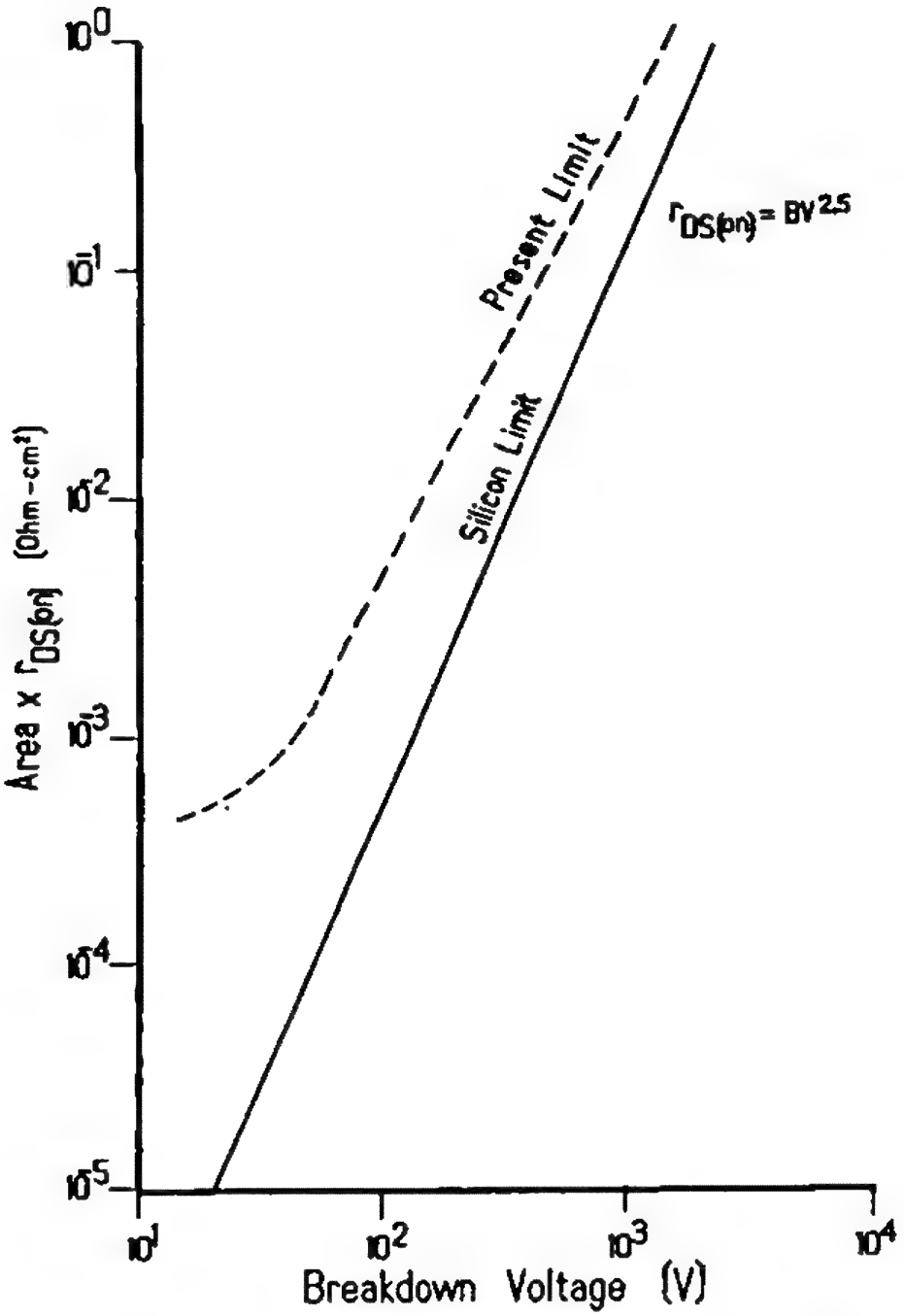

Figure 10.7 The theoretical limit of silicon MOSFET performance, showing the present limit achieved (1987). Note that below 100 V the chip area no longer follows the theoretical limit. This is partially caused by the need for increasingly larger bonding pads (to handle the higher currents) and surface conductor widths to handle the current densities.

10.6 Power DMOSFETs in Linear High-Frequency Amplifiers

Unlike the lateral DMOSFET (see Figure 1.18), the V-groove DMOSFET (see Figure 1.17), because of its construction, exhibits

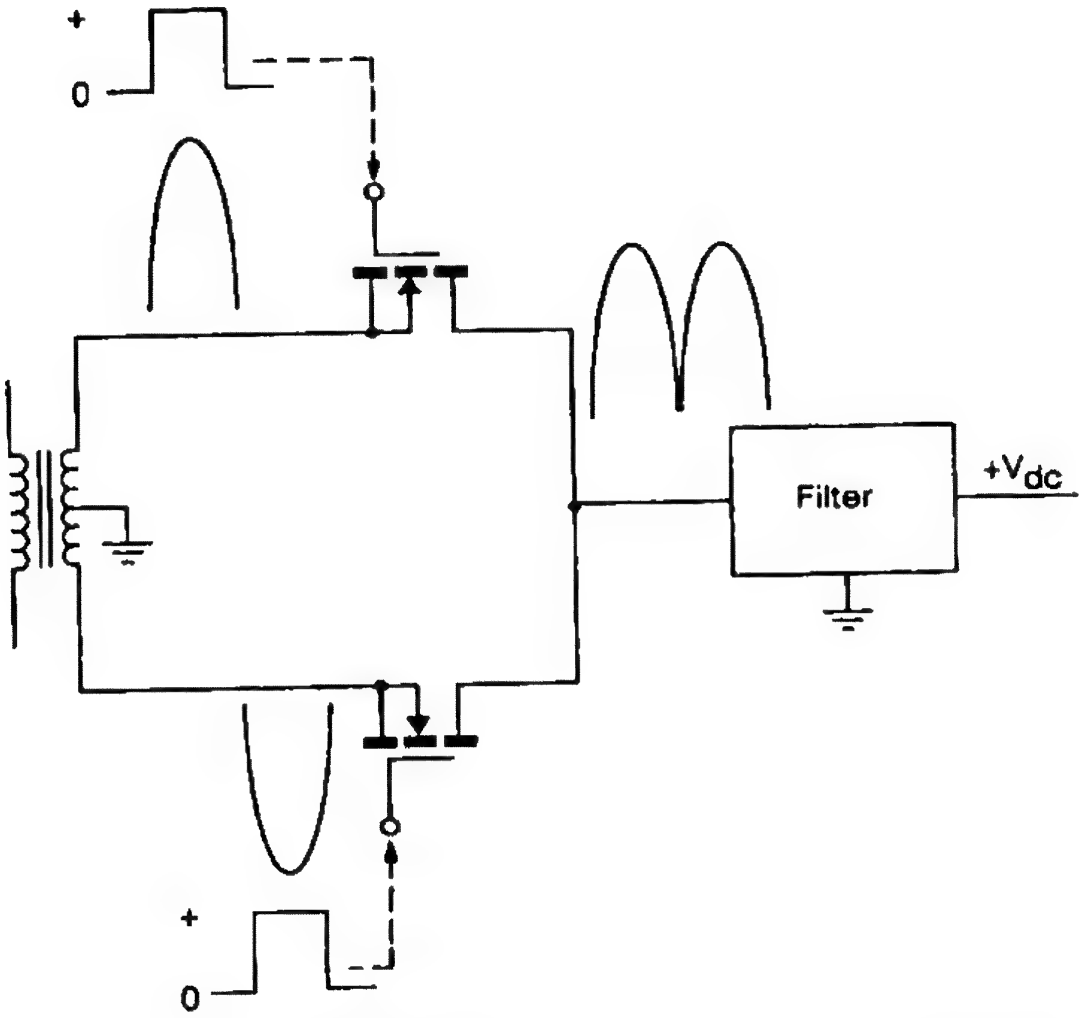

Figure 10.8 DMOSFETs as a synchronous rectifier. Note that the *drains* are common and that the parasitic diodes are arranged for full-wave rectification. The gate drive *must* be synchronized with the rising a-c waveform.

a very low gate-drain capacitance and, therefore, a very low Miller capacitance. Because of the lower Miller capacitance, the V-groove DMOSFET (VMOS) is generally preferred in high-frequency amplifier design. Regardless of whether VMOS or DMOSFET is our choice, to achieve a *linear* response we must guard against any capacitive reactance modulation caused by a varying (sinusoidal or modulated) drain voltage acting on the drain-source capacitance (see Figure 4.19). As we raise the operating voltages, the parasitic capacitances eventually reach an asymptotic state, where any further increase in voltage results in an insignificant change in capacity. To ensure linear performance, we must not operate below this voltage level.

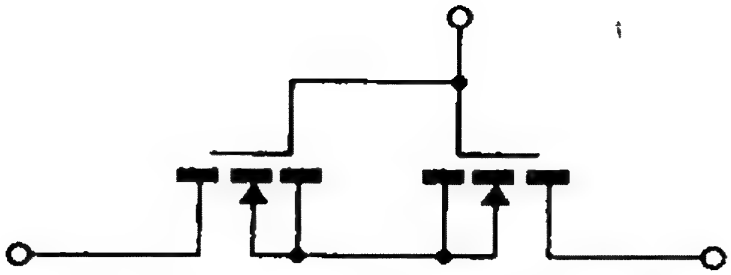

Figure 10.9 Back-to-back DMOSFETs are necessary to enable current control in both directions.

10.7 DMOSFETs as Analog Switches

From earlier study we know that the power DMOSFET conducts in either direction: source-to-drain through the diode, or drain-to-source through the enhanced channel. If we were to implement the DMOSFET as an analog switch, to ensure an effective OFF state we must prevent conduction through the parasitic diode. The simplest scheme is to use a pair of DMOSFETs in series back to back, as shown in Figure 10.9. Such a scheme is quite effective, and high voltages and high power levels can be effectively controlled. Yet there is an important precaution that all too often is forgotten: the maximum gate-to-source voltage specification. If the *peak* analog voltage exceeds $V_{(BR)GSS}$, the DMOSFETs are lost. To avoid the catastrophe, remember to *float* the gate drive. A simple circuit is offered in Figure 10.10.

10.8 DMOSFETs in H-Bridge Motor Drives

Considerable effort has been and is being expended in developing pulse-width modulation (PWM) motor drives using DMOSFETs. Depending on the circumstances surrounding the design, the parasitic drain-source diode's recovery characteristic has, at times, inhibited total success. The basic H-bridge motor drive, shown in Figure 10.11, operates by the successive turn-ON of diagonal pairs of DMOSFETs, 1 with 4, 2 with 3, which alternately switch the current flow through the motor winding.When the conducting diagonal pair of DMOSFETs are switched OFF (for example, 1 and 4) the resulting flyback current is clamped by the parasitic diodes of the alternate diagonal DMOSFET pair

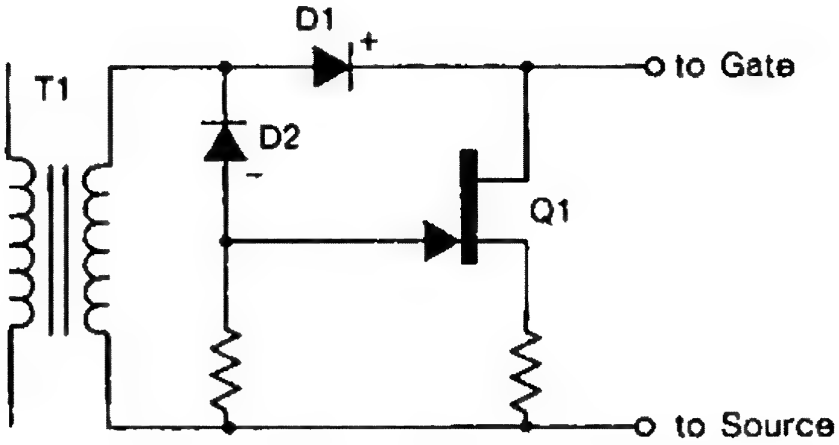

Figure 10.10 Floating gate drive for DMOSFET when the source-to-ground voltage is greater than the gate-to-source breakdown voltage. Diode D1 provides the gate bias; D2 biases Q1 OFF; T1 may be iron core (for low-frequency coupling) or air core (for high-frequency coupling).

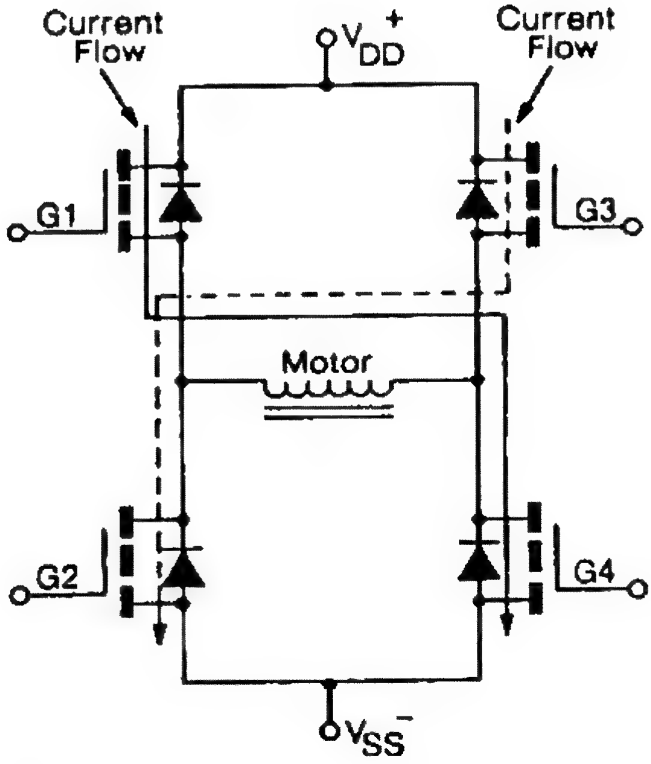

Figure 10.11 Rudimentary DMOSFET H-bridge motor drive showing alternating current flow. Note that the parasitic drain-source diodes also perform as clamping diodes during operation.

(2 and 3). Because of the diode's finite reverse recovery time, if the formerly conducting DMOSFETs are reactivated before full recovery (as might happen when under the control of torque-controlling PWM drives), damaging shoot-through currents as well as damaging slew rates (dV/dt) may result.

An alternative to the quadripolar DMOSFETs would be to replace the upper two (1 and 3) with p-channel IGBTs, leaving the lower n-channel DMOSFETs under the control of the PWM and having the IGBTs control the direction of the motor by their alternate switching. Without the troublesome parasitic diode, the IGBT inhibits shoot-through as well as the potentially damaging dV/dt to the DMOSFETs.

10.9 The Static-Induction Transistor

Although the SIT was developed as early as 1960, the principal source of this transistor in Japan is Tohoku Metal Industries Co., Ltd. Using the trade name Tokin, the manufacturers have not only successfully introduced several devices of rather massive power-handling capability (see Figure 7.10), but also have developed a series of novel switching and linear applications. Because of its ability to perform at high power levels as well as at high frequencies—even into the low microwave region—the SIT may gain a foothold as Western manufacturers tool up for production.

10.10 A Preview of "Smart" Power

As we wind down this introduction to FET technology, we need to be aware of the opportunities for integrating small-signal FETs with large-signal, or power FETs. CMOS and DMOS transistors and DMOSFETs are already found together on a chip. JFETs are commonly found together with bipolar transistors in FET-input operational amplifiers. Perhaps the greatest challenge to manufacturers will be partitioning—that is, the ability to find the common denominator among many diverse applications. Once such an entity has been found, we can either build on it (monolithic integration) or surround it (hybrid fashion) to create new applications.

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Symbol Index

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